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Review On Low Speed Communication Protocols Like SPI, I²C and UART.

Shanthipriya S[1]*, and Lakshmi S[2].

[1]M. TECH VLSI , Sathyabama University, Chennai, Tamil Nadu, India.
[2]Assistant Professor, Faculty of Electricals and Electronics, Sathyabama University, Chennai, Tamil Nadu, India.

ABSTRACT

This paper is mainly based on the survey on low speed communication protocols .SOC consists of processors, interconnects, various subsystems like Modem, GPU, display, sensor and peripheral subsystem. SOC uses peripheral sub system to interface with external chips. These communication protocols can be divided in to 2 categories, one is high speed communication protocols And another is low speed communications protocols. High speed communication protocols are optimized for performance while causing higher power consumption. Low speed communication Protocols are optimized for low power consumption, while they are targeted for low data through put applications. Protocols like I²C ,SPI, UART falls in to this category.

Keywords: SOC, GPU, I²C, SPI, UART

Corresponding author

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INTRODUCTION

The low speed peripheral subsystem includes low speed communication protocols like serial peripheral interface (SPI),inter integrated circuit (I^2C) and universal asynchronous receiver and transmitter. These three protocols are well suited for serial communication. SPI was developed by the company called MOTOROLA. This was derived from the architecture MOTOROLA 68000 microprocessor which announced in 1979.M68HC03 microcontroller was the first microcontroller with SPI bus. The Motorola M68C11 is still available with the same architecture. Though SPI is a external microcontroller bus ,it is used to connect microcontroller peripherals with four wires. For detail specification of SPI the microcontroller data sheet should be read.[1]

Coming to I^2C it was found in1982. The main aim of I^2C is to provide easy way of connection between cpu to peripheral chips. This can be connected as parallel address and data buses. But this leads to lot of wiring on printed circuit boards and glue logic that decode the address bus on which peripherals are connected. philips labs in Eindhoven, the Netherland, invented I^2C in order to make PCB's less complex and simpler. I^2C protocol requires only two wires to connect all peripherals. The speed of I^2C us is 100 kb/s. this was reviewed many times ,then in 1994 they introduced the speed of 400kb/s. This I^2C protocol does not require any license fee for implementation as of october 1,2006. By using "fair open policy" the Philips semiconductor will always demonstrated with I^2C.[1]

UART is a hardware device of the computer. It acts as asynchronous serial communication where speed of transmission and data format can be configurable, It is used in various communication standards such as RS-232,RS-422,RS-485. Generally there are different type of UART like dual UART , Quadruple UART (NXP28L194),octal UART like Exar XR16L788.The basic function of UART is to convert serial data to parallel forms. It will collect the data in the form of bytes and transmit as bit by bit to the other end in step by step manner. When UART is used in between the equipment it will not directly transmit or receive the external signals, they convert logic level signals.[5]

LITERATURE REVIEW

Aviraj Ghanekar (2016) described about the SPI protocols that this protocol is the trendy protocol which is used to.ink peripherals to microcontroller or microprocessor. this can be used 8 or 16 bit data transfer. Generally the SPI protocols uses 4 lines for transmission of data. [2]

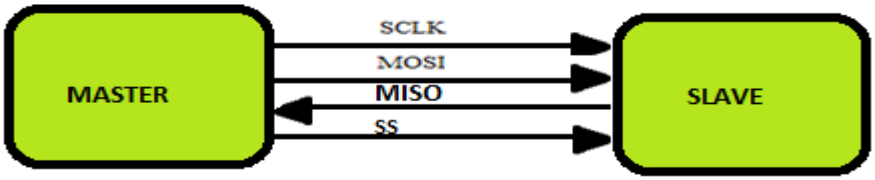

Fig 1: SPI Master and Slave

Figure 1 shows that SPI protocol transmit the data through four signal lines they are SCLK which is so called serial clock which synchronize the data transfer. Then MOSI (i.e) master out slave in where data is transmitted from master device to slave device. Then MISO (i.e) master in slave out where data is get transmitted from slave device to master device. Atlast there is a line called SS which is nothing but slave select line which is operated by master device that which slave device should start communication. When it goes low that particular slave device will get activated. The main key feature is ,it is has independent clock cycles where it can transmit and receive data simultaneously both at the raising and falling edge of the clock. The baud rate of protocol is calculated by using following formula.[2]

i)Baud Rate = Bus Clock /Baud Rate Divisor

ii)Baud Rate Divisor = (SPPR + 1) · 2(SPR+1)

The speed rate of SPI protocols is low or medium which ranges upto 10MHZ.[2]

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M.Sandya(2012) described that SPI bus is used for bidirectional transmission of data by using several modules between microprocessor and slaves. The three important modules of SPI bus are i) Design of clock generation module ,ii)Serial interface module ,iii) Top level module .[3]

In Design of clock generation module the output signal s-clock is produced with various frequency factor of the clock register, where clock signal of the clock generation is the main root from the system clock – wb clk. The odd or even frequency division will be generate for the serial clock of transmission in order to attain reliability. [3] In serial interface module design is responsible for the transmission of data from parallel to serial and serial to parallel. Then comes top level module , the main aim of top level module is to work on smoothy, therefore it requires control word, normal clock generation and transmission module and all these module are designed by using verilog language.[3]

Jayant Mankar (Jan2014) described that I^2C and CAN are the only protocol which is used at software addressing and when compared to CAN, I^2C to protocol design in simple and easy. This communication protocol has two active wires and one ground connection. The two active wires are namely as SCA and SDA. Where SCA is a Serial Clock and SDA is the Serial Data. If in bidirectional in nature and half duplex, where they carry information between the devices connected to bus. Each device have a individual address either for Transmission or reception that depend on function of device. There are various components in I^2C communication like prescale Register, Command Register, Transmit Register and Receiver Register. The Prescale Register is used to convert from high frequency to low frequency by integer division. As immediately when data comes into the Status Register it will wait for command register for commands, according to command it will act. (i.e) either to transmit or Receive data and this data will be transmitted to data I/O register. The I^2C Master Byte Controller are the byte command in which the heart of I^2C communication at byte level. It generates different states by state machine to perform various byte operations. The data I/O shift register component is work with data associated with I^2C for read and write transaction[4] The Master bit controller of I^2C involves bit command controller and clock generator. Here the data is transmitted bit wise into command bit controller from there is will be transmitted and SDA. At the time of reception the process occurs vice versa (ie) first the data comes SDA and then bit controller.I^2C working is based on different stages. The two main signals at I^2C in SDA and SCL.At start condition the SDA line get low and it pull the SCL line low. During stop condition the bus master the SCL line and then SDA line in order to stop. [4]

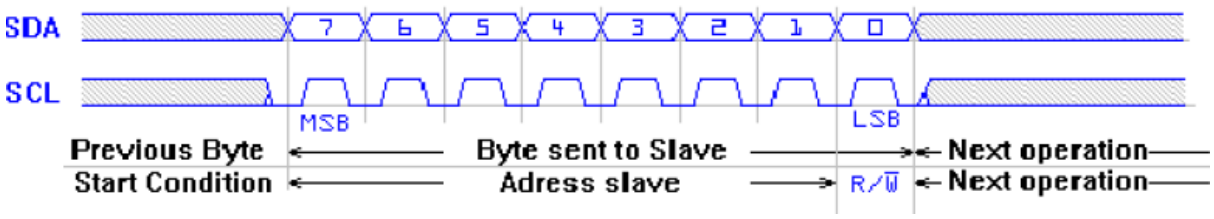

Fig 2: Transmission of a byte to a slave

Figure 2 shows that transmission of a byte to a slave when the start condition occur a byte of data is transmit from master to slave. The first byte will identity the address from slave and rest of the bytes are depend upon regular slave. [4]

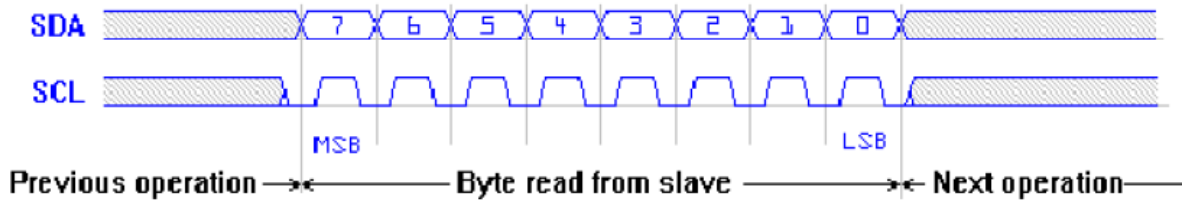

Fig 3: Reception of the byte from a slave

Figure 3 shows Similarly while receiving a byte from a slave device. The slave response to be acknowledge. When the slave Read and Write bit of the address won set to read i.e set to 1. Figure 4 shows that when getting acknowledge (ACK) from a slave it should be acknowledge by the slave for slave device when

an address or data transmitted. On giving ack now from a slave device. The master must acknowledge to the slave device when it receiving data from slave device. If not, NACK signal will send and stop the data transmission. [4]

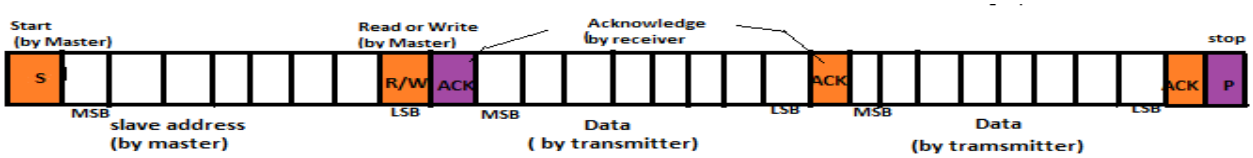

Fig 4: Byte structure

MS.Neha R.Laddha (jan2013)described about serial communication by UART that this protocol is mainly used for serial communication in order to reduce signal distortion because of its simple structure ,and it is effective for long distance communication. The universal asynchronous receiver transmitter is reliable for data transmission and the used for different techniques for it. [6] Figure 5 shows that UART is mainly divided into three sub modules initially the baud rate generator and then a receiver and transmitter. In order to control UART receiver and transmitter the baud rate generator will produce low clock signal which should greater than a baud rate. The UART transmit module transmits the bit through TXD, whereas the UART receiver module will receive signals through RXD.[6] . The design of UART is more reliable, stable and flexible when using FIFO and gives high BGS rate.[7].

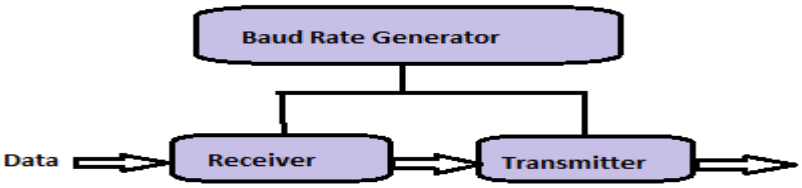

Fig 5: UART Module

As it is full duplex receiver and transmitter, it has inbuilt programming which controls on computer interface to its attached serial devices. The shift register is the main thing for serial transmission. The both transmitter and receiver are said to identical frequency when a baud rate is generated.[8].

Swathi Dubey May 2016 described in Implementation of UART that UART will convert serial to parallel data which has low velocity, short distance and low cost. In order to achieve reliable compact and stable data transmission the UART is designed with very high description language can be integrated into field programmable gate array to achieve error free received data and different frequencies of Baud . The baud rate is calculated by using following formula.[9]

BAUD RATE = NO.OF BITS TRANSMITTED/RECEIVED PER SECOND.

CONCLUSION

This survey is described about working of low speed communication protocols and it will be used to support low speed peripheral subsystem . so a survey has been made to understand the specification of all these protocols. All the papers and journals which are explained and mentioned that how the protocols works in a particular format and what are the rule should be followed while designing these protocols. These designs are used in various electronics applications. From the complete survey the function of these low speed communication protocols are studied which is used for low power consumption.

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