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Review on Performance of Adders for VLSI Applications.

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ABSTRACT

In this paper an extensive study on several adders has been manifested to design VLSI applications. Adder circuits plays a major role to modify or design a multiplier. Imprecise adder is one of the design where used in increasing the performance and power efficiency and approximate adders are for error detection and correction.16T full adders is also used to fast and energy efficient adder. An adder is digital circuit that performs addition of numbers. Approximate adders are widely being used in order to improve performance in error resilient applications. Error detection is done by using probability method. Ripple carry adder are shown which it has better power efficiency, performance speed. Adders are being optimized by using transistor sizing technique in order improve consumption and transistor count. In order to improve the energy efficiency and speed we use a technique i.e. pipelined or parallel structure. Variable latency adders are embedded in order to reduce the average addition time by the help of speculation. Xor-Xnor 1-bit full adder which gives best performance than others circuits. As we take one of the adder to design a multiplier.

Keywords: approximate adder, full adder, multiplier, variable latency adder, ripple carry adder.

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INTRODUCTION

An adder is digital circuit that performs addition of numbers. In many computers and other kind processors, adders are used not only in the arithmetic and logic unit, but also in few other parts of processor and units, where as they are used to calculate the address, table indices, and similar other operations. In Addition usually impacts widely the overall performance of digital systems and an arithmetic function. Adders are also used in multipliers, in DSP to execute various algorithms like FFt, FIR and IIR. Large no. of instructions per second are performed in microprocessors using adders. So, speed and performance of operation is one of most important constraints. Design of more efficient, fastest data path logic systems are one among the most essential areas of research on VLSI. One of the greatest challenges facing in modern VLSI design is to reduce high power consumption.

Many applications can tolerate errors in their arithmetic operations without affecting the end user experience. These futures can be used to design arithmetic circuits which are speed, power efficient and less area, while making a trade of with accuracy of the output. A large number of such applications are involved in media processing, like image, video and audio based applications designed for the use of human interface.

There are many types of adder circuits which has their own specification. In this survey there approximate adder circuit which is used generates exact output on most input combinations, to detect error and error correction. Full adder's circuits are fast and area efficient. Imprecise adders' circuits are for less power consumption and fast processing.

LITERATURE SURVEY:

Pallavi Saxena (2015) is discussing on Brent-Kung adder is much-known logarithmic adder circuit that gives a minimum number of stages from input towards whole the outputs but with asymmetric loading on all middle stages. It is a parallel prefix adder. Parallel prefix adders are not like other class of adder that are based on the way which they use of generate and propagate signals. The expenditure and wiring complexity are low in Brent kung adders. But the gate level depth of Brent-Kung adders is 0 (log2 (n)), so the Speed is lower. Brent Kung Adder has reduced delay as compared to Ripple Carry Adder. The block diagram of 4-bit Brent-Kung adders shown in Fig1

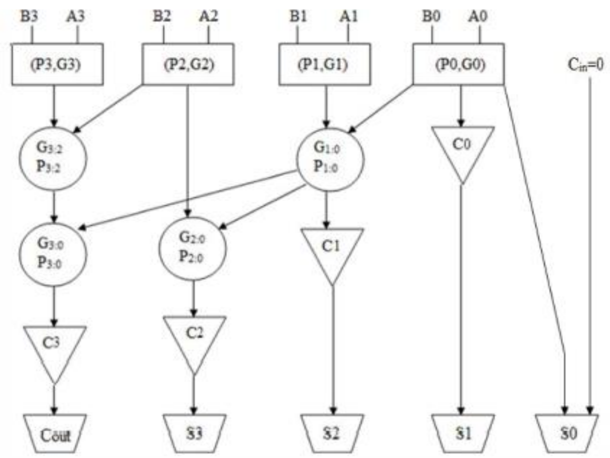

Fig1: Brent-Kung Adder circuit

LINEAR BRENT KUNG CARRY SELECT ADDER

Regular Linear BK CSA is designed by using Brent Kung Adder. Regular Linear KS CSA contains of single Brent Kung adder for Cin=O and a Ripple Carry Adder with Cin=1. It consists of four groups of equal size. Each and every group consisting of single Brent Kung adder, single RCA and multiplexer. Here we use tree structure form in Brent Kung adder to increase the performance speed of arithmetic operation. The block diagram of Regular Linear BK CSA is shown in Fig.2

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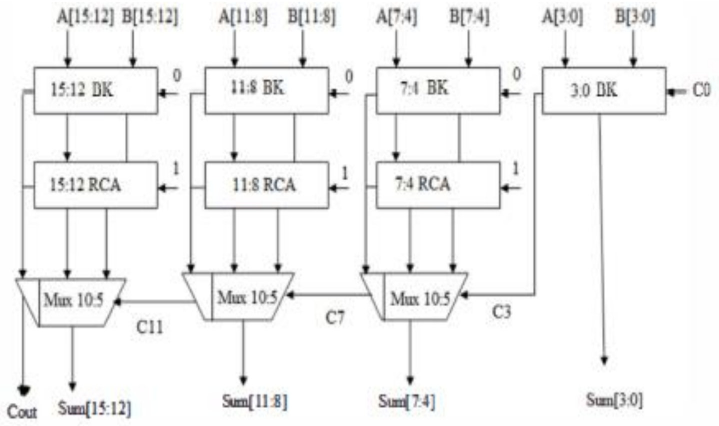

Fig: 2 Regular Linear Brent Kung Carry Select adder

FULL ADDERS

Ebrahim Pakniyat .et.al (2015) they are discussing Full adders circuits are 1-bit.It performs 3-bit addition. Which contains A and B are the inputs and Cin is input carry. Sum and Cout are the result of sum and output carry. Since each of three sub-circuits of full adder can be implemented by using different logics. Shown in fig3

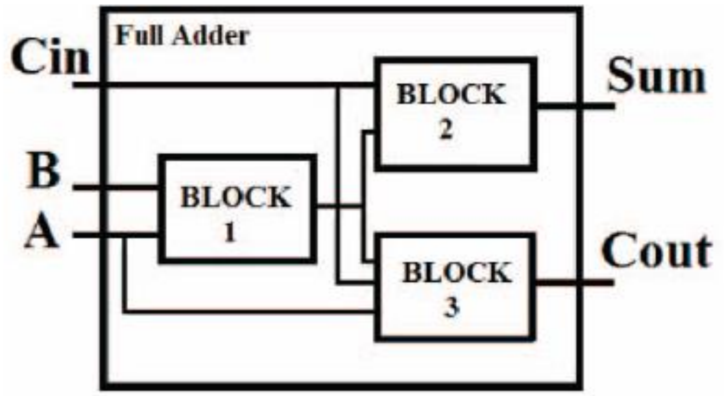

Fig3: Block Diagram Full Adder

Different logics are xor-xor full adder, xor-xnor full adders and xnor-xnor full adder. Shown in fig4

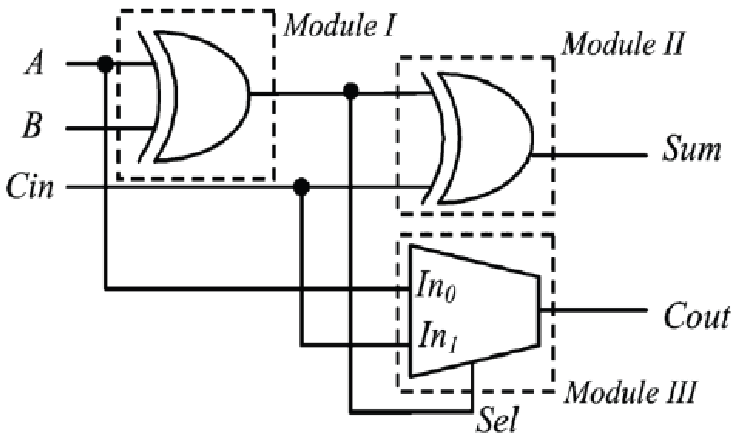

Fig4: XOR-XOR FULL ADDER CIRCUIT

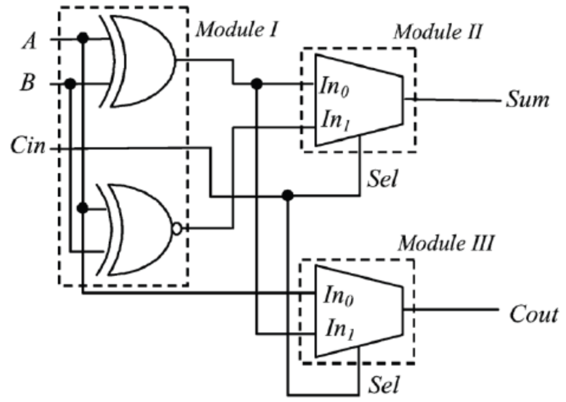

Fig5: CIRCUIT DAIGRAM OF XOR-XNOR ADDER CIRCUIT

Darjn Esposito et.al (2016) are discussing on Variable Latency Speculative Parallel Prefix Adders. A variable latency adder (VLA) reduces average addition time by the help of speculation: the exact arithmetic function is replaced by approximated one, that is faster and gives correct results most of the times.

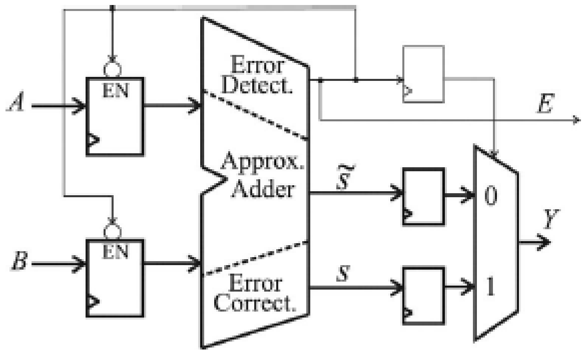

Fig5: Variable Latency Speculative Adder

Sachin Kumar and Chip-Hong Chang (2016) are the Residue number system (RNS) is gaining increasing popularity in the VLSI implementation of application-specific digital signal processors (DSPs). This is in part due to its ability to accelerate and to reduce the power consumptions of crucial and frequently used data path operations by sub word-level parallelism and modularity, and in part due to the ease of realizing modulo operations using the module of the forms 2*n* and 2*n*+ 1.

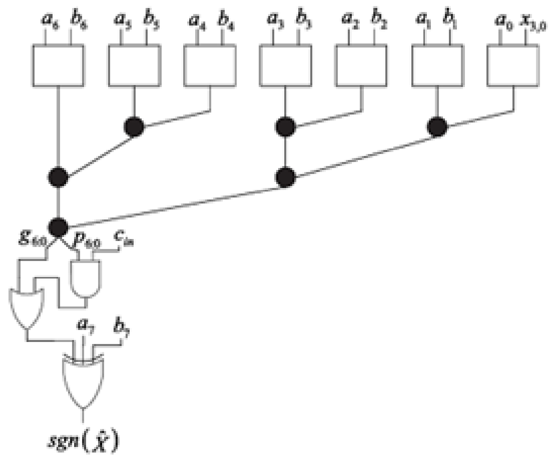

Fig 6 : Simplified prefix adder for n=8

Huazhong Yang et.al (2016) they are discussing on an approximate adder with hybrid prediction scheme and error compensation is presented. Three innovative techniques are proposed to adder design to ensure the property of high energy efficiency and low error output

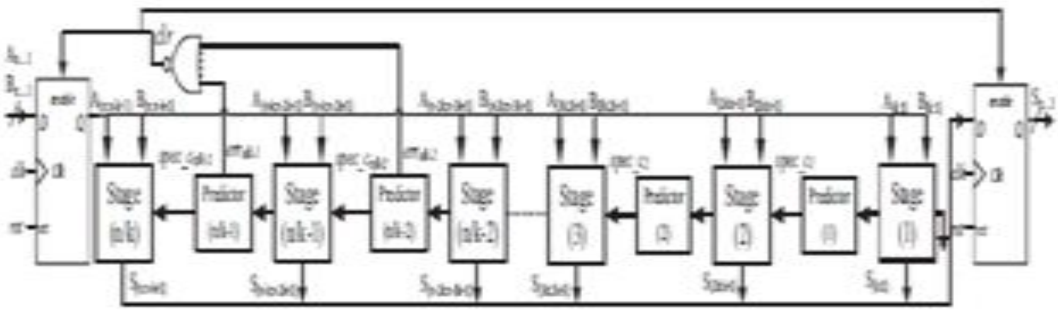

Fig7: General scheme of Proposed Approximate Adder

First, the conventional type RCA is divided into multiple stages which are with series of predictors with one error control method which is based on multistage latency design. Second thing is, in order to decrease the average cycle consumption and the energy consumption, the original prediction design is modified, where the D-Flip-Flops (DFFs) in lower predictors are eliminated to avoid extra clock cycles. Since, the wrong prediction is in lower part that could propagate to higher bits of output and decrease the performance of adder. At last, an error compensation technique is used to further increase the output quality of the unit.

CONCLUSION

An extensive survey has been done for various designs of adder circuit. We have explained briefly about some of the adders. When comes to variable latency adder is one among the adders which reduces power consumption and time lag by parallel speculation. In SFA (single bit full adder) by using depth pipelined architecture the increase the through put. Novel full swing low power 1-bit full adder gives minimum of power consumption, delay and PDP for any voltage input. By using simpler computational building blocks we achieve less energy. By using sub-threshold technology in full adder design there is an improvement in the speed and performance. Improvement through by using suitable predictors to increase output quality, little area and power consumption. By these improvement there are helps in overcome some accepts. When they come in real time, show more impact.

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