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Review on Performance of Nano Spa Processor

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ABSTRACT

In the past few years, several conversions have been made related to asynchronous design frame due to its betterment over synchronous (clocked) systems. In this duration of time, the SPA process was introduced, whose main objective was to focus on power efficiency, lower electromagnetic emissions, adaptability to fabrication, but the performance was a descent. In order to improve the performance, a set of new handshake components were subsequently added which raised the performance by two folds. The advancement in the original SPA processor has led to the existence of an experimental Nano spa. Unlike SPA, the main goal of Nano spa is to improve the performance. After several analyses, it has been found that the performance of the Nano spa can be further elevated. Though the other factors are not assuring,analyses is been made continuously.

Keywords: Efficient Time Delay**,** Nano Spa processors, Optimization, Stability Systems

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INTRODUCTION

Virtually in today's world, almost all the computer systems are synchronous. The main reason for being that is internal timing device which governs the processing. But with the amelioration in the Asynchronous system, the performance has been improved drastically like power-efficiency, low Electromagnetic emissions, and alleviate its adaptability in fabrication Process variation and average-case performance[2]. Asynchronous architectures allows modular design generally with very own attributes. Each subsystem or functional block, without any synchronization can be optimized which simplifies the interfacing. In addition to that, an asynchronous system shows a relatively average performance in comparison with the individual components. Simultaneously, the asynchronous processors also provides decreased power dissipation inherently or shutting down the idle parts of the circuit. Before drafting any architectural overview, concise from the history also interprets about the AMULET processors that is commonly known as the previous version of SFA Processor and had been using the old BALSA synthesis system. This processor came into existence in the year 1993 and its size was about1.0um, similar to ARM 6 which supplies the general speed of 16 MIPS. This device consists of Amulet3i, an asynchronous subsystem comprising an upgraded and re-engineered processor core, similar to ARM9 and includes the Thumb support, tightly coupled 'dual-port' RAM with ROM and an asynchronous DMA controller.

LITERATURE SURVEYS:

Jim. D. Garside et al (2002) described that the amulet3i microprocessor comprises of both RAM and ROM and a tractable DMA controller. The amulet core processor consists of the Harvard memory interface and Von Neumann memory interface. The delay in the amulet core processor can be reduced by using Harvard memory architecture which has the separate bus. This has been implemented in the asynchronous design tools for the area and power management.

Jaggar. D. Seal. D (2002) introduced the ARM instruction and thumb instruction into the Nanospa processor. The Nano spa processor does not back the thumb instruction and the half word transfer. Thumb instruction is an in-built process in the ARM instruction set. ARM v5T ISA has supported the Nanospa processor. Thumb instruction is a 16 bit register and it equals to 32 bit ARM instruction set. The efficiency can be improved by using the ARM instruction[5].

J. Sparse and Steve. B. Furber (2003) delineated the fundamentals of asynchronous design and the working of the handshake circuit components. They used the Muller c element for writing the coding for objects. High level languages were used for the implementation of handshake circuit components in the asynchronous design[1].

W.J. Bainbridge etal (2005) worked on the self-timed circuits that were used to enhance the security to their resistance towards non - invasive attacks. Power analysis and electromagnetic analysis are completely based on the attacks. In this paper they performed the experimental work for the security sensitive devices. Spa processor was executed in ARM v5 ISA. Finally the spa processor has discovered the fabrication process in the smartcard application. Here the dual-rail methodology was used for counting the series of transistor simulation level in the balsa synthesis system.

Q.Y. Zhang and G.Theodoropoulos (2005) presented the techniques like address data and control hazards. In the synchronous design technique clock speed will be increased. The main disadvantage of this technique is the clock inter skew chip. Asynchronous design technique is considered to consume less power and has high performance system. This MIPS processor supports the 32 –bit register in the binary multiplication and division system. This processor works only in the Harvard memory interface and because of that the delay will be reduced in the asynchronous design[3].

S. Taylor and D. Edwards (2008) designed the new handshake circuits for the synthesized asynchronous circuit performances. By implementing the newly designed handshake circuits they have increased the speed of the performance by reducing the latency of control structures. False variable is a new handshake component and it has some data which is operated by its own speed. Without changing the original spa processor they have augmented the performance of Nano spa processor.

L.A. Plana et al (2009) decided to optimize the performance and area of the spa processor. They made use of the handshaking components. This component can be classified in two different ways namely bundle data and dual rail protocols. In this paper, in order to increase the performance, they added the pipeline registers which required the inter stage pipeline to decouple them. Pipeline register can be added in two ways. They are pipeline variables and pipeline buffer modules. Series of transistors level simulation are used in the balsa synthesis system[6]

L.A. Tarazona et al (2011) expressed their ideas on performance of the Nanospa specification. They have enabled both dual rail and bundle data styles in the balsa system. The role of the dual rail is to calculate the power analysis .The bundle data style intended to calculate the timing analysis report. The two techniques used for the significance of performance of the system are Data driven and speculative operation. By using the Dhrystone bench mark they calculated the performance, area, power of the Nanospa processor.

CONCLUSION

A comprehensive survey has been done for various designs and the result of the survey shows that the pipelined structure and the SPA processor was introduced as a fully-automated system that successfully synthesized large and complex designs. Performance was not a major concern for the SPA processor, but the Nano spa was developed with the performance as its main goal. The architecture was built in such a way that the performance can be very well enhanced in the future. Several studies indicate that the progression of Nano spa is mainly about improving the performance and efficiency.

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