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Survey on Different Power Gating Techniques.

A Kirthanaa*, and P Umarani.

Department of VLSI Design, Sathyabama University, Chennai, Tamil Nadu, India.

ABSTRACT

With the advent of latest technologies, the total power consumption of any digital circuit is of great concern. Several researches has been carried out in reducing the leakage and dynamic power consumptions ,so as to increase the self-life of the batteries employed in practical applications. To mitigate the total power consumption in any circuit, ASICs or FPGAs, various conventional power gating techniques has been adopted depending upon the need of the application. Power gating is generally the process of shutting-off power to the idle blocks which do not affect the functionality purpose of the system to which it has been applied. There are numerous power gating procedures available to reduce the total power consumption and this paper provides the detailed survey information about the various power gating techniques which has been proven to produce better result in reducing the total power.

Keywords: power gating, leakage power, dynamic power, area.

Corresponding author

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INTRODUCTION

power dissipation is becoming prime design constraint for VLSI engineers as there is increasing demand for low power, mobile computing and consumer electronics as the battery power increases by 15% every year and the total chip power increases by 35% over the last two decades[16]. As the components are becoming more battery powered, smaller and require more functionality, the requirement of low power consumption is also continues to increase significantly .the reduction of power has to be taken into consideration starting from the design stage of the system physical implementation, circuit level, gate level till the architectural level of implementations. Leakage and dynamic power consumptions are considered to be the major source of power consumption in any circuit .dynamic power consumption mainly depends upon the switching activity of the physical capacitance, thus, minimizing the switching activity offers the possibility of minimizing the power consumption . but, reducing the physical capacitance can also affect the current drive of the circuit making it operate slowly. For CMOS technology down to 130nm technology, the main source of power consumption is dynamic power consumption. Due to scaling process in CMOS technology, leakage power is the significant contributor of total power. During the active and stand by mode , leakage power is dissipated. There are various factors associated with the leakage current includes gate leakage, gate induced drain leakage ,sub threshold leakage and reverse bias junction leakage[12]. Significantly, sub threshold leakage dominates the major source of leakage power consumption. As the scaling process shrinks ,dynamic power consumption has also to be treated with equal importance along with the leakage power.

Selection of proper technology is one of the key aspect of power management in most of the cases. Improving the performance, density and power consumption are the goals behind every technology advancement. But, it is impossible to optimize both leakage and performance at once in any technology . one variant is preferred over the other in any cost as it involves several aspects like oxide thickness, supply voltage , threshold voltage etc.,As technology shrinks more care has to be taken into consideration while mitigating power. basically , clock gating and power gating are the two techniques used for reducing the dynamic and leakage power respectively. For power gating technique to reduce the leakage power consumption , predictive control technique is used. but, at times mis-prediction leads to increased energy consumption of the circuit and hence it is necessary to look at the power delay product of the circuit. Thus, power gating provides the most popular method for reducing the leakage power consumption and it simply implies the process of powering down the unused blocks in any circuit. Power gating is generally implemented with the use of sleep transistor to the selected area of the circuit. There are mainly two types of power gating technique which has been widely used to reduce the leakage power, that includes fine grained and coarse grained techniques[9] . Depending upon the granularity of the structure the type of power gating technique which has to be applied is determined.

LITERATURE REVIEW

In order to establish power gating various procedures have been adopted and below are few of the power gating techniques which have been proposed by different authors across the globe. Assem et al., proposed the concept of dynamically controlled power gating in the FPGA architecture . By this concept ,the selected modules in the FPGA architecture can be powered down at the run time itself and it has been proven that 83% of power saving is possible with the effective area and power trade –off. They have implemented to the number of power gating regions (PGR) and the number of tiles in the PGR indicates the granularity of FPGA architecture. The power state of each PGR can be dynamically controlled ,turned always-on and always-off by configuring to a unique power state. This type of power gating can be applied to any type of tile based configurations. The power state of PGR can be changed by the power control signal which has been configured on before hand with the help of SRAM cell. Thus, by this method idle power dissipation can be brought into control and it is highly flexible to implement in power gating modules at any arbitrary number and they proved that ~8% of energy saving has been achieved by this dynamically controlled architecture when compared to implement with clock gating alone.

CH.Shravan et al.,[2] proposed a power gating technique for the improved charge recovery logic . they have formulated the power gating technique for the asynchronous power gated logic technique that passes the logic function to the next immediate stage which acts as a hand shake signal for the succeeding stages. Thus, during the active mode, they have reduced the leakage currents by providing infinite resistance path by the NMOS transistor in the pull down network . For handshaking to happen separate hand shake controller is

used. Thus, by this method they have achieved power saving upto 82.22% in efficient charge recovery logic system and 92.68% against the static CMOS logic .

Amit ranjan trivedi et al.,[3] proposed a method to achieve trade-off between leakage saving and transition energy overhead by a power gating technique . They have designed a self-adaptive power gating technique that invokes power gating at certain specified condition particularly when the leakage saving is more than the transition energy overhead. This also enables the dynamic configuration of circuit from the power gating and non-power gating modes. The break-even cycle of a power gated domain can also be tracked while performing self adaptive power gating method.Thus,self adaptive power gating achieves lower area and power overhead while enabling process, temperature and history based adaption. Thereby reducing the leakage in digital system.

Marie et al.,[4] proposed a method to reduce the dynamic power consumption of FPGA .by directly detecting the activity of each look-up table using the detectable features of asynchronous architectures, the advance detection of the arrival of data can be predicted. It has been found that the delay required for the waking up of a logic block and the total power dissipation of the asynchronous circuitry has been greatly reduced by avoiding the unnecessary switching. Lesser area overhead has also been achieved when compared with the existing methodology. Thus the four phase dual rail encoding is proven to be suited for the look-up tables as it occupies lesser area while LEDR encoding has been used to achieve high throughput and low power in switching block.

Karthikeyan et al.,[5] analyzed the asynchronous circuits granularity and implemented a asynchronous fine grained power gated logic. The asynchronous fine grained power gated logic perform operations only if the logic blocks are more active and the idle logic blocks are not powered thereby reducing the negligible leakage power at run time. The handshake controller provides the control the subsequent stages of the circuitry. The asynchronous fine grained power gated logic in the power gating region pipeline uses enhanced c*element in its handshake controller. Such that it will reduce the leakage dissipation by entering into sleep mode early.

Rajagopalan et al.,[6] propose a autonomous power gating technique for the reconfigurable FPGA design. As, the FPGA's consume high dynamic and stand by power ,it employs autonomous fine grained power gating. In this method, each look-up table is provided with a sleep transistor and also a sleep controller. So that when the look-up tables are not active ,they can be put into sleep mode immediately . as FPGA's are composed of numerous look-up tables in its architectures ,powering down the idle look-up tables help in reducing the total dynamic power consumption of the circuit and the LEDR encoding is also used to control the data flow at the input and output of FPGA blocks. Thus, by selectively driving the functional units into the low leakage mode when they are idle, power reduction is achieved.

Yogeshkumar et al.,[7] used a four step power gating technique to reduce the ground bouncing which occurs normally during the conventional power gating procedures. Generally, during the process of power gating, the switching activity of the circuit increases and it drives the circuit to suffer from ground bouncing. Besides ,controlling the bouncing, it also controls the transition energy overhead during the transition period and wake-up time of the transistors. the wake-up transition of a power gated circuit in a controller is employed in a four step manner. For reducing the voltage swing and discharge current in the noise limiting stage ,pre boosting and post boosting current technique is applied to control the wake-up time . They have proved that by this method power saving up to 73% is possible and 20% reduction in the bounce noise is achieved with the three stage power gating technique.

Kwangok et al.,[8] proposed a technique to power gate an active core when it stalls during the long memory access . they have reduced the leakage power by power gating a core while it is stalled waiting for a resource . to vary the cores wake-up delay ,a programmable two stage power gate switch design is formulated while maintaining voltage noise limits and leakage power savings. They have also modeled the power distribution network of the processor and its effect on the memory access power gating on neighboring active cores . They have also proved that ~38% of power saving is potentially possible by perfect power gating on memory access and they have practically implemented in a counter circuitry to prove that more than 20% of the power can be saved.

Pradeep et al.,[9] analyzed the power gating for the FPGA look-up tables. The look-up tables consist of SRAM array cells and multiplexers. Each FPGA is made up of numerous look-up table . By applying the fine grained and coarse grained power gating technique to separate look-up tables of the FPGA ,dynamic power consumption due to the switching activity has been greatly reduced . they have mainly focused on the SRAM cells of the FPGA and coarse grained power gating can virtually cuts off the power supply to every part of the SRAM cell array. they have proven that the coarse grained power gating can save more leakage power when compared with the fine grained power gating technique and yield approximately 99% and 81% leakage power saving respectively when compared with the modules before applying the power gating technique.

Sin-yun chan et al.,[10] dealt with the leakage power consumption of the structures ASIC. To curtail the sub-threshold leakage, power gating is used to disconnect the logic blocks from power network . They have applied the power gating to the configurational logic block of the structured ASIC using the existing standard cell design tools. For the configurable logic block they have implemented distributed sleep transistor network, cluster based power gating and the fine grained power gating technique to analyze the leakage power reduction. They have produced result with 8% area overhead and 17% delay over head for52% leakage power reduction. Thus, reducing the leakage power in the standard ASIC is proven to be difficult when compared with the structural ASIC and its successor FPGA's.

SURVEY SUMMARY

The literature review on the section (II) mainly focuses on the various power gating techniques adopted by different authors for specified application .There are numerous methods adopted to reduce the leakage power in the design. They have either applied fine grained power gating or the coarse grained power gating technique in general for most of the design. Fine grained power gating is applied when the granularity of the system is more and it encapsulates the switching cell as a part of the logic cell. It mainly suffers with the excessive area over head issue and fewer timing issues. In coarse grained power gating technique, the power gating has been applied to the cluster in general . Here the power gating transistor is used as a part of power distribution network rather than the standard cell. Coarse grained power gating also produces timing issues but it is negligible when compared with the fine grained power gating procedure and it also provides lesser area over head.

Apart from this two well known technique, a dynamically controlled power gating technique [1] is used to power down the idle blocks of the architecture during its runtime. Other power gating operation can be powered up or down during the execution time whereas dynamically controlled power gating can switch between the power states during the run time itself. Thus, they have defined three states of operation which includes always-on, always-off and dynamically controlled state.

For asynchronous circuits, hand shake controllers are used to pass the signal to the next subsequent logic and the prediction of the input data arrival is possible . the switching activity of the asynchronous circuit [4] is brought into control which helps in reducing the power. For FPGAs and reconfigurable architectures , self-adaptive[3], autonomous power gating techniques are used. It mainly focuses on the look-up tables of the reconfigurable FPGA architectures as it is the primary element in any FPGA architecture . Thus, depending upon the type of application and the need behind the architecture design, various power gating techniques can be used to reduce the leakage power but establishing the trade-off between area, power and delay is the tedious task. Fine grained power gating incurs excessive area over head among the other types of power gating while dynamically controlled power gating[1]incurs lesser area over the existing conventional power gating methods. When delay and timing issues are of concern, coarse-grained power gating produces better result as per the studies.

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