Design and analysis of Efficient Scaled-down magnetic full adder using Magnetic Tunnel Junction.

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ABSTRACT

Low power consumption, non-volatility, high endurance are the key features offered by memory and logic design of Hybrid MTJ/CMOS. The issue of leakage power is resolved and the benefit of non-volatility is gained by using Hybrid MTJ/CMOS. An enhanced design for magnetic full adder using MTJ is designed and it is observed that power consumption of the circuitry is less when compared with existing method. An enhanced design for magnetic full adder using MTJ is implemented using HSPICE tool and it is been observed that the overall reduction in area and power of about ~17% and ~12% respectively.
Keywords: Magnetic Tunnel Junction, Leakage power, spintronics Magnetic full adder.

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INTRODUCTION

With the growing demand for high performance computing, the evolution of technology in the field of VLSI has contributed to a great extent. The trade-off between area, speed and power consumption are the key parameters that plays a vital role in the system design effecting the overall performance of the system. Reduction in size of transistors results in minimum power consumption and increased speed because of the reduced parasitic resistance, capacitances and inductance.

Spintronic is the study of intrinsic spin of electrons which can be detected as the magnetic field that has two orientations namely, parallel and antiparallel spin [8]. This has given rise to the nano-structured device called magnetic tunnel junction(MTJ).MTJ can be constructed by using two ferro magnets separated by a thin insulator, which exhibit a magneto resistive effect called tunnel magneto resistance[6].The tunnel magneto resistance can be given by the relation, TMR= $(\Omega_{ap}-\Omega_p)/ \Omega_p$. where Ω_{ap} is antiparallel resistance, Ω_p is the parallel resistance. A Magnetic full adder has been constructed by studying the property of ferromagnetic material present in the mtj. As MTJ is capable of reducing the leakage power present in any circuitry, it is capable of reducing the same without deteriorating the property of a full adder and thus gives rise to the magnetic full adder. We will compare the existing full adder with the proposed full adder and analyse the betterment of parameters like speed, area and power consumption.

Existing Magnetic FullAdder

Full adder is an essential block of the ALU for any processors. Improvement in the Speed and chip density of a processor is achieved with an effective design of full adder.
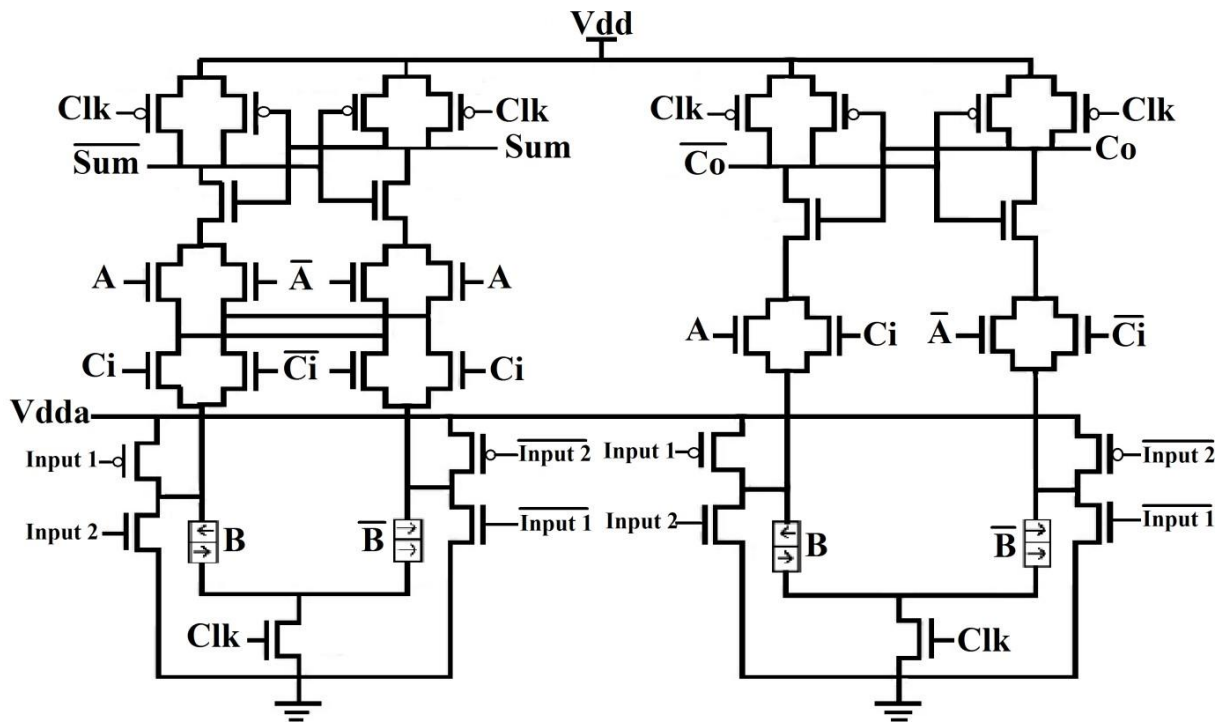

Figure 1: Magnetic Full adder circuit with sense amplifiers

Spin transfer torque based magnetic tunnel junction (STT-MTJ) is chosen to bridle the invariable power problem. Fig 1.1 is a STT-MTJ circuit with inputs namely A, Ci, B and outputs Sum and Co.

$$SUM = ABCi + ABCi + ABCi + ABCi \qquad (1)$$
$$Co = AB + ACi + BCi \qquad (2)$$

Input B relates to volatile storage STT-MRAM. Pre-charge sense amplifier (PCSA) is utilized for detecting the configurations of embedded MTJs and amplifying to logic signals which gives the appreciable

sensing reliability and power efficiency, on the other hand maintaining high speed performance (200ps) compared with other sense amplifiers [1]. The pre-charge Sense amplifier circuit consist of couple of inverters which acts as a amplifier, a discharge sub-circuit and a pre-charge sub-circuit. When the CLK signal is high, the circuit will be pushed into the EVALUATION mode. During the course of evaluation, the Sum and Carry outputs are generated based on the present state inputs and the values are stored when the CLK turns low resulting to HOLD mode. The current sense amplifier holds opposite logical value on sum, $\overline{sum}$ and Co,$\overline{Co}$. The truth table for the magnetic full adder[2] is given as Table-1.

Table 1: Truth table of MFA

A	B	Ci	Sum	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

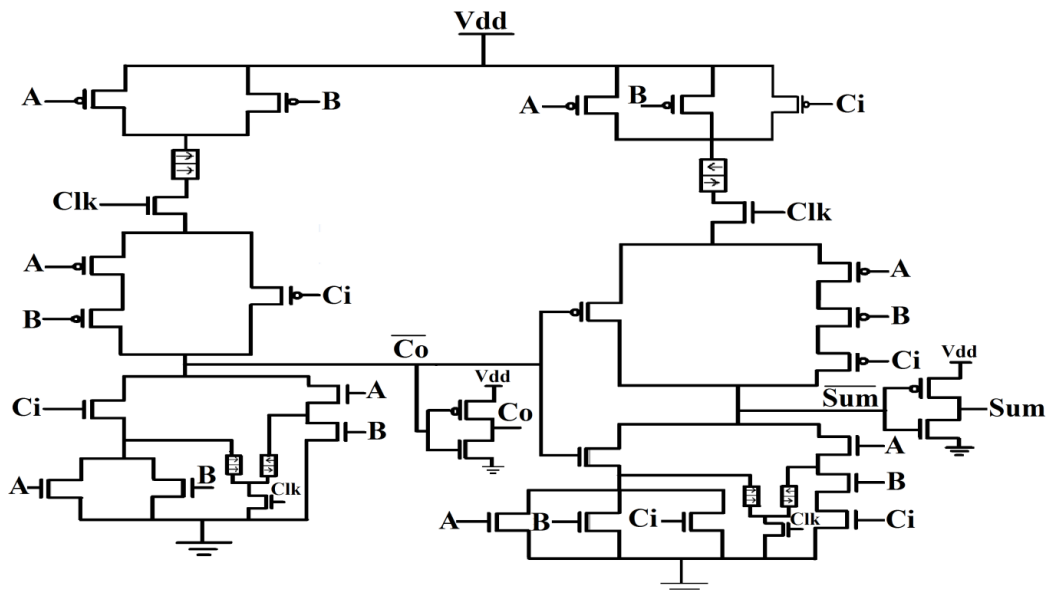**Efficient scaled-down Magnetic Full Adder**

Figure 2: Efficient scaled-down Magnetic Full Adder circuit

Figure -2 shows a proposed efficient scaled down magnetic full adder circuit having three inputs A, B and Ci and two outputs Sum and Co. The total number of transistor count has been scaled down when compared with the existing work and also leakage power has been brought into great control. After the node by node analysis of circuit, high leaky nodes are identified which in turn lead to power leakage, even when the circuit is idle. Magnetic Full Adder works on the basis of normal full adder. For the sake of reduction in leakage, implementation of MTJ is done. In Sum logic, the MOS tree relates directly to the logic relationship of three inputs A, B, and Ci, can simply take up to the general structure with two complementary STT-MRAM cells. In the existing system, the number of MTJ present is four and in the proposed system, the number of MTJ represent is six because MTJ can reduce the leakage power issue.

RESULTS AND DISCUSSIONS

Figure-3 shows the simulation of transient hybrid of STT-MFA. It is performed by using STT-MRAM compact models and CMOS 130nm design kit. The time-dependent characteristic of outputs (SUM and Co) establishes the function of full addition. An example operation is shown: inputs A=1, B=0, Ci=0, sum is 1 and no carry. For the operation A=1, B=0, Ci =1, the result is 0 and the carry is 1.The output of the existing magnetic full adder is shown below,
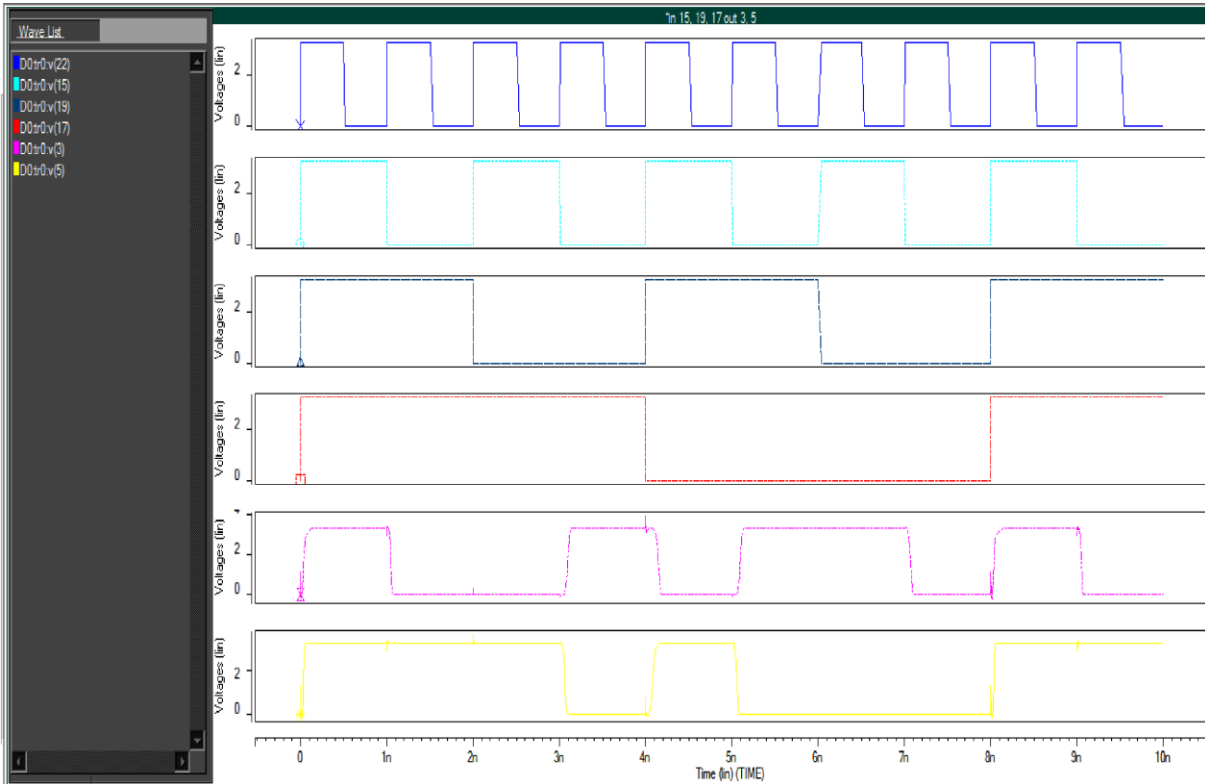

Figure 3: Output for existing magnetic full adder

Figure-4 illustrates the transient hybrid spice simulation of proposed efficient scaled-down magnetic full adder. It is done using MTJ Equivalent models introduced above and CMOS 130nm design kit. The sum and carry output logics are obtained based on the functionality. For instance, for the operation "A"=0, "B"=1, "Ci"=0, the result is "1" and yields no carry .For the operation "A"=1, "B"=0, "Ci"=1, the result is "0" and the carry is "1".
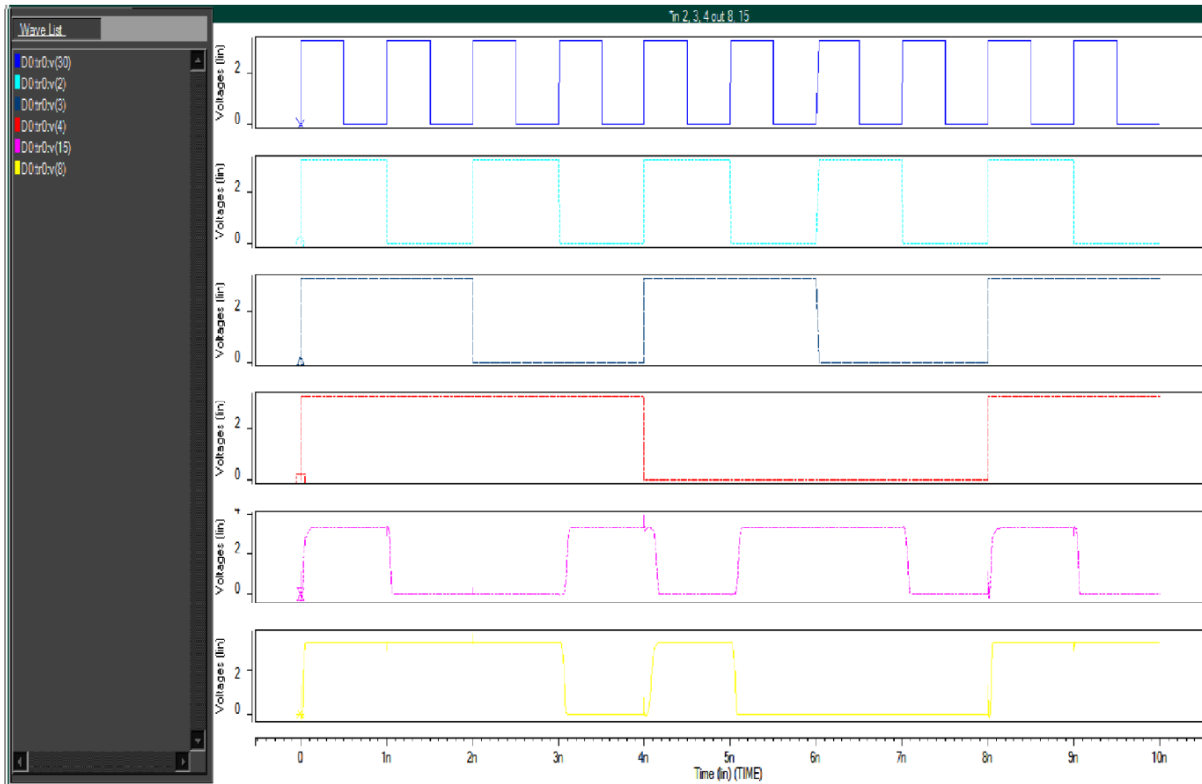
Figure 4: Efficient scaled-down Magnetic Full Adder

The below table-2 shows the power , delay ,area and power delay product analysis of the existing magnetic full adder and efficient scaled down magnetic full adder using 130nm technology. It is been observed that proposed design power consumption, area as well as delay are less when compared with the existing one. Similarly, the table 3, 4 shows the power , delay, area and power delay analysis of MFA using 90nm and 45 nm technology respectively.

Table 2: Using 130nm Technology

Types	Area (No. of transistors)	Power mw	Propagation Delay ns	Power delay product pJ
Existing method	34	0.1017	6.274	0.638
Proposed method	28	0.0997	6.24	0.622

Table 3: Using 90nm Technology

Types	Area (No.of transistors)	Power mw	Propagation Delay ns	Power delay product pJ
Existing method	34	0.0711	6.204	0.470
Proposed method	28	0.0688	6.178	0.425

Table 4: Using 45nm Technology

Types	Area(No.of transistors)	Power mw	Propagation Delay ns	Power delay product pJ
Existing method	34	0.0545	6.124	0.333
Proposed method	28	0.0412	6.078	0.251

CONCLUSION

In this paper, efficiency of MTJ is analyzed. Efficient scaled-down Magnetic Full Adder has been designed and its performance parameters are been compared with the existing methodology. It is been observed that, the implementation of MTJ in any combinational and sequential logic circuit as well as memory circuit will consume comparatively less leakage power and it plays a pivotal role in reducing the chip area.

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