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Design and Simulation of Modified Symmetric and Asymmetric Multilevel Inverter.

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ABSTRACT

Multilevel inverters offers less distortion and less electro-magnetic interference compared with other conventional inverters. But it utilizes a large number of power electronic switches to achieve higher output levels. The main objective of this paper is to analyze the performance of the modified single phase multilevel inverter with reduction in number of switches. This inverter topology can produce9- level output voltage waveform during symmetrical operation and 17- level output voltage waveform during asymmetrical operation with only eight switches and four DC voltage sources. Since the proposed topology uses less number of components, the overall size and cost of the inverter is reduced considerably. The performance of the inverter is analysed for different switching angles and the results are presented. The simulation is done using Simulink /MATLAB software.

Keywords: *Mulilevel inverter, Symmetric, Asymmetric, THD, Switching angle*

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INTRODUCTION

Multilevel inverter plays a significant role in the field of modern power electronics[1-2].The various commonly used multilevel inverter topologies are diode clamped, flying capacitors and cascaded H-bridge multilevel inverter [3-5]. The various advantages of multilevel inverter over conventional inverter includes less harmonic distortion, low dv/dt stress, low switching frequency and less electromagnetic interference [6-7]. The main drawback of the multilevel inverter is it requires large number of switches and associated gate driver circuit [8-9].

Many topologies of multilevel inverter have been proposed by various researchers over the last few decades. This paper proposes a new inverter topology with minimum number of switches. The proposed multilevel inverter uses four sources and eight switches. The proposed inverter can operate in both symmetric and asymmetric modes. The different modes of operation of the inverter is explained in Section-2. The different methods of calculating the switching angles are discussed in Section-3. The simulation results obtained using MATLAB/Simulink are presented in Section-4. The conclusion is presented in Section-5.

PROPOSED MULTILEVEL INVERTER

The topology of the proposed inverter is shown in Fig.1. It consists of four sources and eight switches of equal rating. It can produce 9-level output voltage during symmetrical operation and 17-level output voltage during asymmetrical operation.

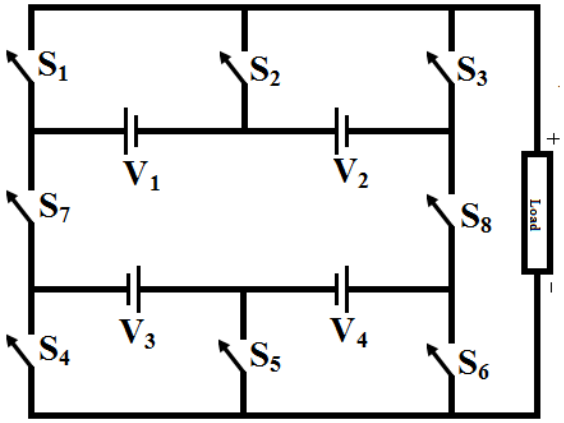
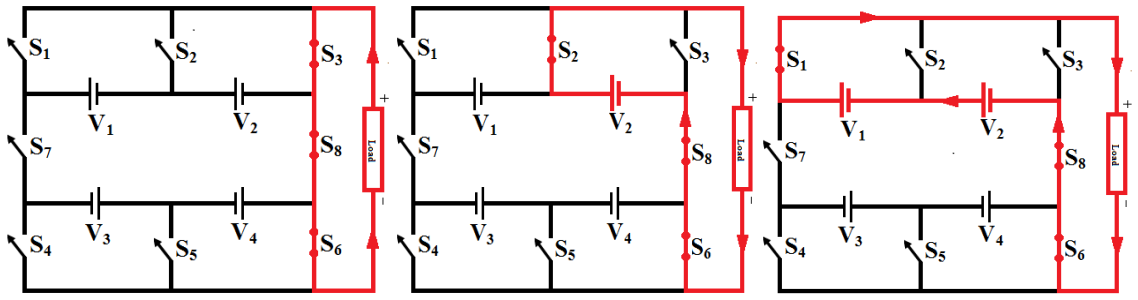


Figure 1: Proposed Multilevel Inverter



(a) *(b)* *(c)*

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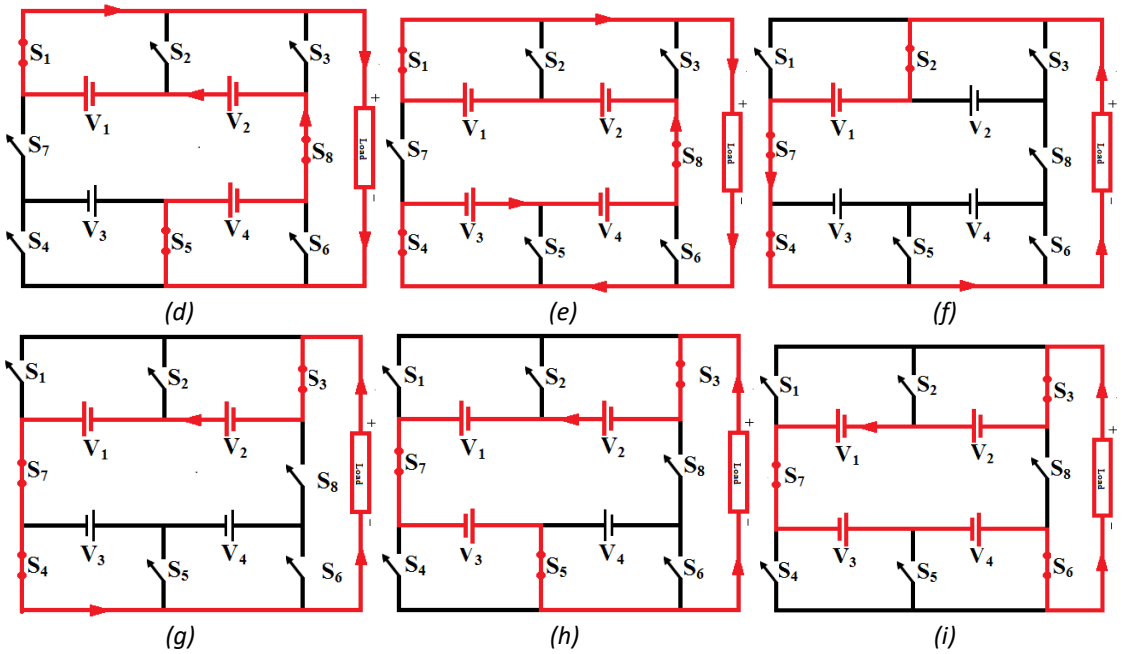

Figure 2: Modes of Operation.

The different operating modes of the inverter during symmetric operation is shown in Fig. 2. In this, Fig. 2(a) shows mode-0 operation, where 0V is obtained across the load. Fig.2(b)-2(e) shows the positive modes of operation, where the voltage obtained across the load is positive.

Fig.2(f)-2(g) are negative modes of operation, where the voltage obtained across the load is negative. The switching states during the symmetrical operation of the proposed multilevel inverter is given in Table 1.

Table 1: Switching states for symmetrical operation

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output Voltage
Mode - 0	0	0	1	0	0	1	0	1	0
	1	0	0	1	0	0	1	0	
Mode - 1	0	1	0	0	0	1	0	1	V_2
Mode - 2	1	0	0	0	0	1	0	1	$V_1 + V_2$
Mode - 3	1	0	0	0	1	0	0	1	$V_1 + V_2 + V_4$
Mode - 4	1	0	0	1	0	0	0	1	$V_1 + V_2 + V_3 + V_4$
Mode - 5	0	1	0	1	0	0	1	0	$-V_1$
Mode - 6	0	0	1	1	0	0	1	0	$-(V_1 + V_2)$
Mode - 7	0	0	1	0	1	0	1	0	$-(V_1 + V_2 + V_3)$
Mode - 8	0	0	1	0	0	1	1	0	$-(V_1 + V_2 + V_3 + V_4)$

The switching states during the asymmetrical operation of the proposed multilevel inverter is given in Table 2.

From the table, it is clear that the ON state switches (i.e., conduction switches) to achieve any level of output voltage will be equal to 3 for the proposed inverter topology. This will considerably reduces the switching losses of the inverter. The comparison of the proposed inverter topology with the other existing topologies is given in Table 3. The parameters used for the comparison are number of dc

voltage sources and the total number of switches. It is seen that the proposed inverter uses minimum number of switches to achieve higher level output voltage as compared with other inverter topologies.

Table 2: Switching states for asymmetrical operation

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output Voltage
Mode - 0	0	0	1	0	0	1	0	1	0
	1	0	0	1	0	0	1	0	
Mode - 1	0	1	0	0	0	1	0	1	V_2
Mode - 2	1	0	0	0	0	1	0	1	$V_1 + V_2$
Mode - 3	0	0	1	0	1	0	0	1	V_4
Mode - 4	0	1	0	0	1	0	0	1	$V_2 + V_4$
Mode - 5	1	0	0	0	1	0	0	1	$V_1 + V_2 + V_4$
Mode - 6	0	0	1	1	0	0	0	1	$V_3 + V_4$
Mode - 7	0	1	0	1	0	0	0	1	$V_2 + V_3 + V_4$
Mode - 8	1	0	0	1	0	0	0	1	$V_1 + V_2 + V_3 + V_4$
Mode - 9	0	1	0	1	0	0	1	0	$-V_1$
Mode - 10	0	0	1	1	0	0	1	0	$-(V_1 + V_2)$
Mode - 11	1	0	0	0	1	0	1	0	$-V_3$
Mode - 12	0	1	0	0	1	0	1	0	$-(V_1 + V_3)$
Mode - 13	0	0	1	0	1	0	1	0	$-(V_1 + V_2 + V_3)$
Mode - 14	1	0	0	0	0	1	1	0	$-(V_3 + V_4)$
Mode - 15	0	1	0	0	0	1	1	0	$-(V_1 + V_3 + V_4)$
Mode - 16	0	0	1	0	0	1	1	0	$-(V_1 + V_2 + V_3 + V_4)$

Table 3: Comparison of Total Harmonic Distortion

Topology	Number of DC sources	Number of DC switches	Levels	
			Symmetric	Asymmetric
Cascaded	4	16	9	21
Ref. [10]	4	11	9	9
Ref. [11]	4	10	9	13
Ref. [12]	4	10	9	15
Ref. [13]	4	12	9	13
Proposed inverter	**4**	**8**	**9**	**17**

CALCULATION OF SWITCHING ANGLES

In this paper, two different methods of calculating the switching angles are analysed.

Method - 1

In method-1, the switching angles are determined by using the following equation:

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$$\theta_i = i\frac{180^0}{N} \quad \text{where}, i = 1, 2, 3..., \left(\frac{N-1}{2}\right)$$

Here, the switching angles are averagely distributed over the range 0–90°.

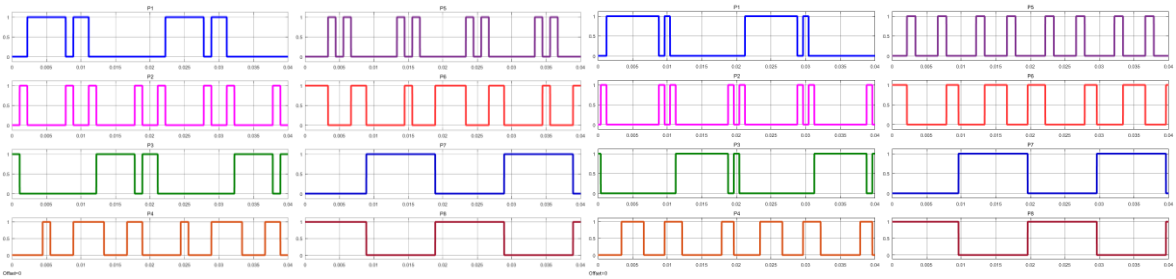
Method - 2

The method-2 gives better output voltage waveform. In this method, the main switching angles are determined by,

$$\theta_i = \sin^{-1}\left(\frac{2i-1}{N-1}\right) \quad \text{where}, i = 1, 2, 3....\left(\frac{N-1}{2}\right)$$

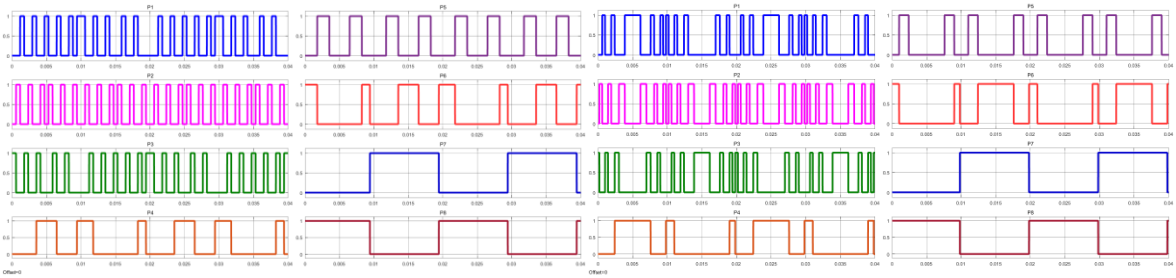
Where, N = Number of output levels.

The switching angles corresponding to the period 0 to 90° are called as main switching angles. For N-level inverter, there are (N-1)/2 main switching angles [14]. The switching pulses obtained using different methods are shown in Fig. 3 and Fig.4.



(a) *(b)*

Figure 3: Switching Pulses for symmetric case (a) Method 1 and (b) Method 2.



(a) *(b)*

Figure 4: Switching Pulses for asymmetric case (a) Method 1 and (b) Method2.

SIMULATION RESULTS

The simulation results of the proposed multilevel inverter are presented in this section.

Symmetrical Case

In symmetrical case, all voltage sources have equal magnitude. In the simulation analysis, the magnitude of the DC voltage sources are considered as $V_1 = V_2 = V_3 = V_4 = 25V$. The maximum voltage obtained as 100 V (i.e., $V_1 + V_2 + V_3 + V_4$). The nine level output voltage obtained for different switching methods are shown in Fig. 5.

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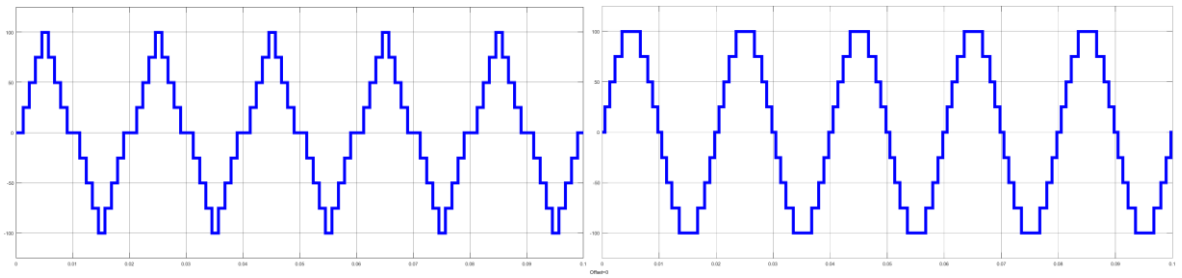
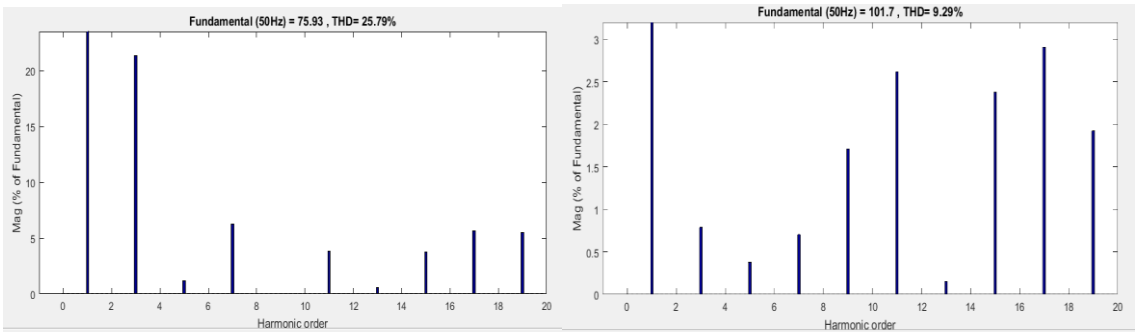


(a) *(b)*

Figure 5: Nine level Output Voltage (a) Method 1 and (b) Method 2.



(a) *(b)*

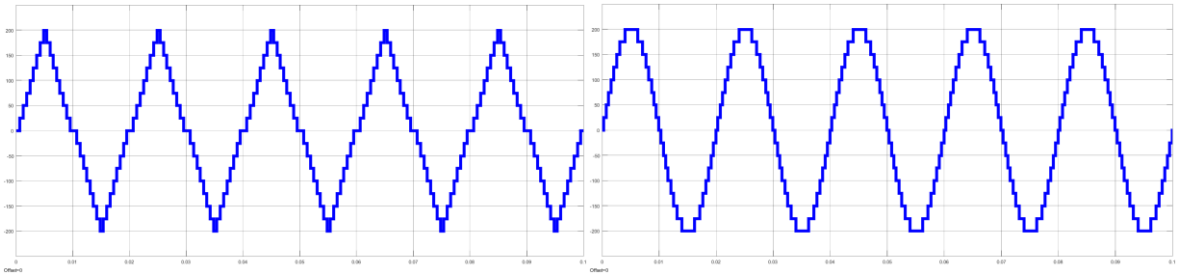
Figure 6: FFT Analysis (a) Method 1 and (b) Method2.

The FFT analysis of the nine level output voltage waveform for different switching method are shown in Fig. 6.

The simulation result shows that the THD of the output voltage waveform for the switching method - 2 is less as 9.29% when compared with the method-1.

Asymmetrical Case

In asymmetrical case, each voltage sources have different magnitude. For simulation analysis, the magnitude of the DC voltage sources are considered as $V_1 = V_2 = 25V$ and $V_3 = V_4 = 75$ V. The maximum voltage obtained as 200 V (i.e., $V_1 + V_2+V_3 + V_4$). The 17-level output voltage obtained for two different switching methods are shown in Fig. 7.



(a) *(b)*

Figure 7: Output Voltage (a) Method - 1 and (b) Method 2.

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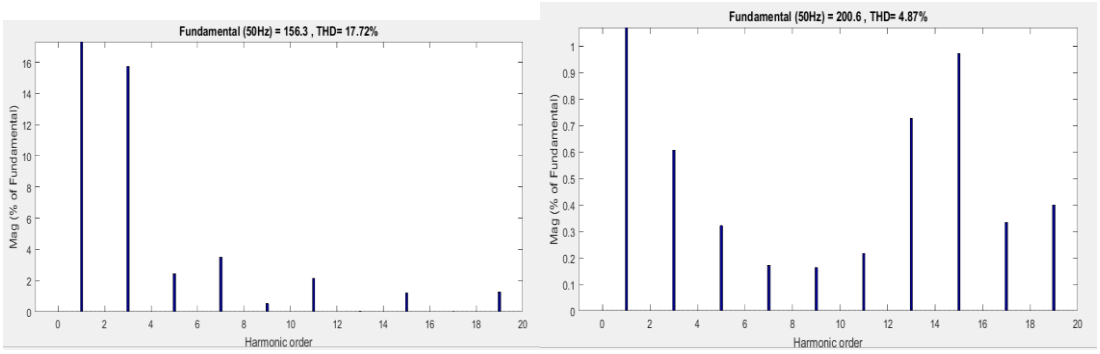

(a) *(b)*

Figure 8: FFT Analysis (a) Method1 and (b) Method2.

The FFT analysis of the 17- level output voltage waveform for different switching method are shown in Fig. 8.The simulation result shows that the THD of the voltage waveform for the switching method - 2 is also less as 4.87% during the asymmetrical operation when compared with the method-1. The comparison of THD results are given in Table 4.

Table 4: Comparison of Total Harmonic Distortion

Case	THD (%)		Output Level
	Method-1	Method-2	
Symmetrical	25.79	9.29	9
Asymmetrical	17.72	4.87	17

Table 5: Comparison of Total Harmonic Distortion

Case	THD (%)			
	Method-1		Method-2	
	Proposed	[14]	Proposed	[14]
Symmetrical	25.79	25.37	9.29	8.37
Asymmetrical	17.72	17.55	4.87	5.02

Table 5 shows the comparison of the THD of the output voltage waveform with the available reference.

CONCLUSION

This paper proposed a new inverter topology with minimum switches. The main advantage of this inverter topology is it uses only four DC voltage sources to achieve 9- level output voltage during symmetrical mode of operation and 17-level output voltage during asymmetrical mode of operation. The two different methods are used to calculate the switching angles and the results are compared. The simulation analysis and the corresponding results are presented in this paper. The result shows that the switching angles obtained by method - 2 achieves less THD compared with method - 1 for both symmetric and asymmetric operation.

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