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Review on CSLA design using Sub Threshold Adiabatic logic techniques.

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ABSTRACT

Digital sub threshold logic circuits can be operated for applications in the ultra-low power end of the design spectrum, where presentation is of minor importance. A subthreshold digital circuit manages to satisfy the ultra-low power condition because it uses the leakage current as its effective switching current. This minute leakage current, however, limits the maximum presentation at which the subthreshold circuit can be operated. Sub-threshold CMOS theory is a technique which can moderate the power consumption to lower than threshold voltage specified and adiabatic logic circuit is a technique to reduce energy intake by suppressing the voltage applied to the resistance of the circuit. This paper gives brief survey to propose that sub threshold adiabatic logic the design of implementation of carry select look ahead adder CSLA.

Keywords: power consumption, sub threshold, adiabatic logic, CSLA..

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INTRODUCTION

Power consumption is rapidly becoming a limiting factor in integrated circuit technology as device sizes shrink. Applications such as wireless sensors, RFID tags, and similar devices have only a very small amount of power available to them, and must be designed to use a minimum of energy. Computer processors have massive amounts of power available, but can fail or become permanently damaged if the energy they dissipate causes severe heating. In an attempt to address these concerns, we have tested the effectiveness of two low-power techniques, sub-threshold biasing and adiabatic charging in the design The continuous growth of recent mobile and portable devices and applications has affected a tremendous thrust for low power circuit design. Various methods and methods, such as voltage scaling, clock gating, etc. have been applied successfully in the medium power, medium presentation region of the design spectrum for lower power consumption. Nevertheless, in some applications where ultra-low power consumption is the major requirement and performance is of secondary importance, a more aggressive approach is necessary. Operating the transistors of a digital logic in the subthreshold region has recently been proposed to achieve ultra-low power consumption. A subthreshold digital circuit manages to satisfy the ultra-low power requirement because it uses the outflow current as its effective switching current. This minute leakage current, however, limits the supreme performance at which the subthreshold circuit can be operated. The subthreshold circuit is thus suitable for definite applications which do not oblige very high act.

Related Works

Robust Subthreshold Logic forUltra-Low Power Operation

Source: - IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 9, Issue: 1)

In this we deliberated two novel subthreshold logic families.A new control circuit for the stabilization of subthresholdcircuit is also discussed in detail. Both VT-sub-CMOS andsub-DTMOS logic families show superior robustness and patienceto temperature and process variations than that of orderedsubthreshold CMOS logic. VTsub-CMOS logic can be willinglyimplemented in twin-well progression technology, but it requiresadditional circuitry for stabilization. In contrast, sub-DTMOSlogic does not require any additional stabilization circuitry butcan only be implemented in triple-well process technology.The additional rise in area and process difficulties forsub-DTMOS logic is compensated by its higher operating frequency while sustaining comparable energy/switching as regular subthreshold CMOS logic. DTMOS has been successfullyimplemented in both SOI [9] and bulk Silicon .VT-sub-CMOS logic, however, has better control on substrate bias.

Analysis and Design of an Efficient Irreversible Energy Recovery Logic in 0.18-nm CMOS

Source: - IEEE Transactions on Circuits and Systems I: Regular Papers (Volume:55 , Issue: 9)

Adiabatic techniques have been effective means to power minimization in deep submicron VLSI systems. In this paper, we discussed a newly developed ERL family termed CEPAL for low-power design. The proposed logic style outperforms those currently demonstrated in irreversible energy recoveryliterature in terms of several aspects. In addition to the summary of prior works, we analyzed CEPAL in detail, and elaborated relative strength and weaknesses of it *vis-a-vis*one of the known subthreshold logic styles. Specifically, we presented the adeptness of the DFFs made up of QSERL and the projected logic style. Since the impact of leakage on CEPAL is
of trifling importance, low- devices can be introduced so as to minimize the non-adiabatic loss, enabling higher circuit functioning. Such low- devices have been existingin theprocesses 0.25 m and beyond.

Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply

Source: - Proceedings of 1997 International Symposium on Low Power Electronics and Design.

The suggested clocked adiabatic logic (CAL) drives from a singlephase power-clock supply. The test chip, a chain of inverters, is implemented in a 1.2 _m CMOS technology. Operation of the logic and its energy

consumption are measured for adiabatic operation using an outer power-clock generator or using a simple on-chip power-clock generator. These results are compared to the energy intake measured in non-adiabatic operation when thechip is powered from a dc voltage source. Tentativeresults show tenfold energy savings in the clock range from 1 MHz to 5 MHz andsignificant savings at clock rates up to 40 MHz, with power-clock generation included. The CAL ability to operate from either ac powerclock supply or from a conservative dc supply opens further potentials for energy-efficient operation in a very wide range of throughput rates by linking adiabatic and nonadiabatic modes of operation.

A 0.25 V 460 nW Asynchronous Neural SignalProcessor with Inherent Leakage Suppression

Source: - IEEE Journal of Solid-State Circuits (Volume:48 , Issue: 4)

As the supply voltage is scaled near or below the device threshold, dramatic increases in leakage and variability severely limit digital processor performances. In this paper, we present robust and energy-efficient computation architecture by employing an asynchronous self-timed design methodology. The proposed strategy allows for an adaptive adjustment to latency variations, and supports for an inherent leakage minimization under process variations and changing operating conditions, all of which are major issues in scaling regimes that favor major reduction in supply voltages. Circuit techniques specifically for leakage minimization are aggressively employed at both the logic and system levels. The prototype asynchronous neural signal processor demonstrates robust operation down to 0.25 V while consuming only 460 nw. Compared to the traditional synchronous approach, the asynchronous design reduction in power. Moreover, the self-timed operation alleviates the impact of variations on processor performance. Therefore, the asynchronous design exhibits a better statistical characteristic of power performance than the synchronous counterpart. These results demonstrate that in addition to soliciting better transistors and fabrication technology, leakage and variability issues can be tackled at the circuit and system levels with novel timing schemes and circuit innovations.

Dynamic Threshold MOS transistor for Low Voltage Analog Circuits

Source: - International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882 ICRTIET-2014 Conference Proceeding, 30-31 August, 2014

Based on measured data available, we have established a new small-signal equivalent circuit model that has an additional current source gmbVbd to express body effect correctly. Using this model, we planned the body contribution of the DTMOS in low voltage analogcircuits (<0.6V).The small signal model for DTMOS device offered in this paper is for long channel. DTMOS can be considered to be one of the most capable devices for low power analog/RF circuits.

A 24GHz CMOS VCO with DTMOS Technique

Source: - Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference

A 24 GHz voltage-controlled oscillator considered in IBM 90nm standard CMOS technology is presented. This VCO innovatively adopts Energetic Threshold MOSFET (DTMOS) structure in its cross-coupled pair transistors to attain larger transconductance. Forward biasing of Body-Source junction advanceaugments overdrive voltage by minimizing threshold voltage. Tail current source is distant to achieve depleted supply voltage. Post-layout simulation shows power dissipation to be less than 2mW and phase noise to reach -102.8dBc/Hz at 1MHz offset

Analysis of Low Power, Area- Efficient and High Speed Fast Adder

Source: - International Journal of Advanced Research in Computer and Communication Engineering Vol. 2, Issue 9, September 2013

Power, delay and area are the essential factors in VLSI design that limits the presentation of any circuit. This work presents a simple approach to reduce the area, delay and power of CSLA architecture. The conventional carry select adder has the disadvantage of more power consumption and occupying additional

chip area. The planned SQRT CSLA using common Boolean logic has low power, less delay and condensed area than all the additional adder structures. It is also little bit faster than all the other adders. In this technique, the transistor count ofprojected SQRT CSLA is condensed having less area and low power which makes it simple and effective for VLSI hardware implementations.

Low Power High Speed SQRT Carry Select Adder

Source:- IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 3 (Nov. - Dec. 2012), PP 46-51

In this paper, a modified 40-bit SQRT CSLA has been suggested for data path circuit (MAC unit) for low power DSP application. Modified CSLA has reduced the power as contrast with usual CSLA with slightly increase in delay. The decrease in the number of gates of this work offers great advantage in terms of area and power. The compared results also show that the modified SQRT CSLA has lower power-delay product (PDP). Hence, the proposed CSLA architecture is better in terms of PDP which leads the better utilization of the DSP processor.

Modified Low-Power and Area-Efficient Carry Select Adder using D-Latch

Source: - International Journal of Engineering Science and Innovative Technology (IJESIT) Volume 2, Issue 4, July 2013

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the excessive advantage in the decline of area and also the total power.The altered CSLA reduces the area and power when compared to steady CSLA with increase in slow downby the use of Binary to Excess-1 converter. This paper suggests a scheme which diminishes the delay, area and power than regular and modified CSLA by the use of D-latches.

CONCLUSION

In this we made a survey that overall power dissipation will be reduced and the transistors count will be reduced half the amount. Where in existing system, we used CMOS logic gates in CLA adder .but for the decrease in power we used Subthroshold Adiabatic technique in CSLA adder in this the analysis of SAL-based 4-bit CSLA are given to show the workability and the feasibility of the proposed logics.

REFERENCES

[1] H. Soeleman K.Roy ,B. C. Paul. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2001; 1:90-99
[2] D. Maksimovic , V. G. Oklobdzija , B. Nikolic ; K. W. Current " Proceedings of 1997 International Symposium on Low Power Electronics and Design 1997 ; 1:323 - 327
[3] Tsung-Te Liu and Jan M. Rabaey IEEE Journal of Solid-State Circuits 2013; 4: 897-906
[4] VandanaNiranjan, AkankshaSingh, Ashwani Kumar nternational Journal of Scientific Research Engineering & Technology (IJSRET) 2014; 1: 26-31
[5] H. Lv, He Qian Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference 2010; 3: 746 - 748
[6] Pallavi Saxena1 , Urvashi Purohit , Priyanka Joshi International Journal of Advanced Research in Computer and Communication Engineering 2013; 9: 3705- 3710
[7] Partha Mitra , Debarshi Datta IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) 2012 ; 3 : 46- 51
[8] Veena V Nair International Journal of Engineering Science and Innovative Technology (IJESIT) 2013; 4 : 375 - 382