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Survey on Low power ALU design by using Modified GDI Technique in Microchip application.

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ABSTRACT

Power dissipation has a foremost impact while we are scheming any circuit. Since this factor plays a chief role in deciding the competence of the designed circuit i.e. why in this paper we are proposing a plan for sequential circuits so that we can diminish the power dissipation. Power dissipation which in turn reduces the whole power dissipation of CPU. In this paper, gives an overview of a Survey on Designing ALU circuits by using gate diffusion input(GDI Technique) and Modified GDI Technique, which gives foremost better results with respect to power consumption, speed and area. The proposed design consists of GDI adder based and mux circuits. By using low power 1-bit full adder in the applications of ALU, the area and power are significantly reduced to more than 50% compared to conventional design and 30% is associated to communication gates. So, the design is ascribed as an area efficient and low power ALU. In this, ALU consists of 2x1 multiplexer, 4x1 multiplexer and full adder is designed using the following logical operations, such as OR and AND operation etc. and arithmetic operations, as SUBTRACT and ADDITION. Etc. GDI cells are used in the design of multiplexers and full adder which are then connected to base on ALU block diagram.

Keywords: Static Power Consumption, Dynamic Power Consumption, Area, ALU, GDI Technique.

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INTRODUCTION

ALU is one of the main constituents of microprocessor. They use fast dynamic logic circuits and have prudently enhanced structures. Its power ingesting explanations for a substantial portion of total power intake of data path [1].ALU also contribute to one of the uppermost power-density sites on the processor, as it is clocked at the highest speed and is kept eventful most of the time resulting in thermal hotspots and shrill temperature gradients within the core. Power dissipation is affecting profoundly the power which is converted to heat and then steered or radiated away from the device. Electronic and electric devices can have a borderline on the current they can securely handle that is not an electronic limit, but a fleshly one. For occurrence, a transistor may be able to knob a certain amount of current, but it is good to set a lower current grade because the die gets too hot. Dissipation is usually restrained in watts, and uses Ohm's law calculations for power. Most of the Very Large Scale IC (VLSI) solicitations, Full adder circuit is a useful building block and most precarious factor of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every multifaceted computational circuit entails full adder circuitry. The entire computational block power consumption can be condensed by implementing low power techniques on full adder circuitry. From different existed base papers more than a few full adder circuits based on different low power techniques have been proposed targeting. We have designed ALU in dissimilar way by using GDI cells to implement multiplexers and full adder circuit. The output and input sections consist of 2x1 and 4x1 multiplexers and ALU is fulfilled by using full adder.

RELATED WORKS

A Novel Low Power, High Speed 14 Transistor CMOS Full Adder Cell with 50% Improvement in Threshold Loss Problem

T.Vigneswaran, B.Mukundhan, and P. Subbarami Reddy

The enactment of many larger circuits are toughly depends on the presentation of the full adder circuits that have been recycled. The new improved 14T adder circuits obtainable in this study are good candidates to build these big systems, such as high concert multipliers with low power consumption. In this paper, we have presented a new improved 14 transistor adder cell to build full adders using only 14 transistors. Based on our extensive simulations, we accomplished that our new adders guzzle considerably less power in the order of micro watts and have 45% higher speed and reduces 50% threshold loss problem associated to the previous different types of Transistor adders. With the help of this adder cell, we can project an effective and high performing multiplier unit. In future, this kind of high speed and lowpower adder cell will be used in designing the digital FIR filter and its applications in various fields.

Power and Delay Optimization of 1 Bit Full Adder using MTCMOS Technique

SonamGour, Gaurav Soni, Swati S.Kumar

The presentation of digital systems in VLSI design be contingent largely upon the enactment of full adder employed in such systems. The presentation of full adder contrasts as the technology scaling is familiarized. In this work, HSPICE simulation of full adder is completed at 32nm and 45nm technology using MTCMOS technique to shrink the delay and power dissipation in the full adder design. The simulation outcome shows lesser power consumption of 98.3% in 32nm and 99.1% in 45nm as related to conservative full adder. And also, the delay is reduced to 21% for sum output and 25% for carry output in 32nm. In 45nm, advancement in delay is achieved by 26% for sum output and 29% for carry output.

A Novel Low Power Energy Recovery Full Adder Cell

R. Shalem, E. John and L. K. John

They offered a novel low power and transistor count static energy-recovering full adder and equated its performance against three other full adder cells for area, delayand power consumption. The three full adder cells for evaluation against SERF adder were selected renewed literature on the subject of low power design. Simulation and analysis studies were achieved on 2-bit and 8-bit ripple carry adders. The anticipated

SERF adder design was proven to be superior to the other three designs in power dissipation and area, and second is to the circulation delay only to the DVL adder. The amalgamation of low transistor and power count makes the new SERF adder cell a feasible option for low power design.

Design and Implementation of Area Optimized ALU using GDI Technique

Akshay Dhenge, Abhilash Kapse, Sandeep Kakde

The traditional GDI and CMOS techniques are used in the designing of ALU is discussed first. An area optimizing technique is introduced and the components with GDI technique are implemented. Later the evaluation between the number of transistor used in old and GDI design of ALU is done. And in the demo it is shown that this GDI design evidently reduces the number of transistor and also to optimize the area of ALU as well with increase in its working speed.

Minimization of Transistors Count and Power in an Embedded System Using GDI Technique

Madhusudhan Dangeti , S.N.Singh

GDI technique is implemented for Basic Logic Gates and some Digital circuits. Comparisons are made between GDI, standard CMOS and some pass transistor logics. The analysis shows that the GDI technique is a novel and an operative technique for decreasing power consumption and the Transistor count which will efficiently decreases the size of the chip. GDI will allow high density of Fabrication. As now a day's chip area is actual important constraint. With respect to chip area, power consumption and transistor count, GDI technique is significantly profitable over other techniques

Modified GDI Technique - A Power Efficient Method for Digital Circuit Design

Pankaj Verma, Ruchi Singh and Y. K. Mishra

In this paper an approach is presented for diminishing power consumption for digital circuits at the logic style level and DC and Transient study of basic logic gates has been done using Mod-GDI logic style. All Simulations are performed through PSPICE grounded on 0.18µm CMOS technology, and outcomes shows the power characteristics of Mod-GDI method of low power digital circuit design. Simulation results shows up to 45% saving in power-delay invention in Mod-GDI. Mod-GDI method allows understanding of a broad variety of multilayered logic functions only by means of 2 transistors. Mod-GDI gates lower the transistor amount and in turn the silicon area needed when compared to standard static CMOS and Domino CMOS based approaches. The leakage power and switching power of Mod-GDI gates is lower than the traditional logic styles. The problem in fabrication of GDI gates in standard nano-scale CMOS process is overwhelmed by connecting the sources of pMOS and nMOS to VDD and GND respectively in Mod-GDI logic style. The problem of threshold drop is not a very serious issue in deep sub-nm regions. The Mod-GDI logic style based design adopts interruption of inverter to alleviate the problem of signal degradation during propagation. This proposed logic style is analyzed to feat the low power and high speed potential feature of Mod-GDI based circuit applications. The comparison between our analysis and prior works indicates that one of this logic styles for small power digital design does deliver many advantages. In short, the proposed Mod-GDI logic style based designs can be taken a better alternative in future. For the period of the desktop PC design and portable age VLSI design efforts have paying attention primarily on optimizing speed to appreciate computationally exhaustive real-time functions such as video compression, gaming, graphics etc. As a result, semiconductor ICs that successfully integrated a variety of complexes signal processing modules and graphical processing units to meet up computation and entertainment demands. As these solutions have addressed the real-time problem, they have not addressed the cumulative demand for portable operation, where mobile phone needs to pack all this without consuming much power. The severe limitation on power dissipation in portable electronics applications such as smart phones and computers must be encountered by the VLSI chip designer while still meeting the computational requirements. At the same time as wireless devices are quickly making their way to the consumer electronics market, a key design restriction for portable operation that is the total power consumption of the device must be taken into account. So for this purpose reducing the total power ingesting in such systems is significant because it is advantageous to maximize the run time with minimum requirements on weight allocated to batteries, size and battery life.

CONCLUSION

Power consumption in CMOS circuit is classified in 2 categories: static power dissipation and dynamic power dissipation. In today's CMOS circuit's static power dissipation is negligible and it is not considered when compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by $P = C_L f V^2_{DD}$. The power supply is directly related to dynamic power. The number of power supply to ground connections is decreased in GDI implementation which reduces the dynamic power consumption. With Using GDI technology designing of an ALU consumesless area and less power consumption.

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