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FPGA Implementation of ASK, BPSK and QPSK Modulator Using Hardware Co-Simulation.

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ABSTRACT

Modulation techniques such as ASK, BPSK, QPSK and other higher order modulation can be easily simulated by using matlab/ simulink and xilink system generator. The block set designed in the xilink automatically generate the code from library files and Xilinx. The hardware co-simulation can be perform with the help of HIL (Hardware-in-loop) and by system generator, which facilitate to dump the developed code or generated code into the hardware and to obtain the output. The time saved by working with these types of high level programs is a real advantage of this proposed work. The ASK, BPSK and QPSK System will be design and implement successfully with the help of Matlab\Simulink and Xilinx\System Generator and the code generated from system generator has been simulate using ISE 14.3 and FPGA design as well as implement on many devices like spatran ,vertex, kintex etc. using Verilog Hardware Description Language can be perform using this process. The observed results can be analyse with real time applications such as satellite communication and video conferencing. Finally, the power consumption of the proposed modulation techniques has been enhanced and compared with existing methods.

Keywords: QPSK, BPSK, FPGA, ASK

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INTRODUCTION

Nowadays, Wireless communication is a prominent area in the field of communication owing to the increasing demand particularly in communication connectivity driven by wireless data and cellular telephony applications. Wireless communication systems need high data rate for transmit information efficiently. Various parameters contribute to achieve goal in this field and one significant parameter is modulation technique. Modulation methods capable to enhance data transmission rate within the same range of bandwidth [1]. Quadrature Phase Shift Keying (QPSK) is one of the most important modulation techniques among others. It is developed from the part of Phase Shift Keying (PSK) modulation method. QPSK has been widely utilized for satellite communication system, wireless local area network communication, video conferencing and various forms of digital communication under a Radio Frequency (RF) carrier [2, 3]. Moreover, QPSK transmit only low rate symbol rather than other digital modulation methods such as Quadrature Amplitude Modulation (QAM) 64 and QAM 32, but it consume only less power and less complex circuit in receiver end [4]. In QPSK modulation, the amplitude and frequency remain unchanged. In contrast, the phase varies with respect to the input data. The quadrature in QPSK refers four different states which are illustrated by a group of 2 bits input. These states can be in the form of 00(0), 01(1), 10(2) and 11(3) as shown in Figure 1.The first and second bit refers in-phase (I) and quadrature (Q) components respectively.

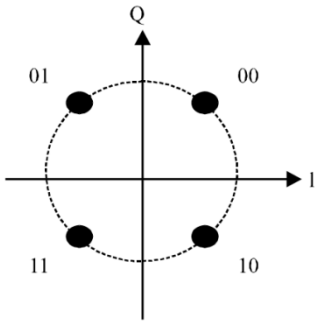

Figure 1: Group diagram for QPSK

The QPSK modulation is developed from two separate Binary Phase Shift keying (BPSK) signals that can be combined into single signal. In spite of this, in QPSK the transmission of data has been improved while the Bit Error Rate (BER) upon the signal to noise ratio (SNR) is sustained at the same level with the actual BPSK [5, 6]. The two times the bit period is the symbol period of QPSK, $2T_b = T_s$, but in the case of BPSK signal both bit period and symbol period is same as mentioned $T_b = T_s$. Kang and Elamary et al. [7, 8] proposed the QPSK digital signal in full domain can save time and cost for long time leads to enhances the wireless data immunity upon surrounding noise.

PROPOSED MODULATION TECHNIQUES

ASK MODULATION

Amplitude shift keying - ASK - in the context of digital communications is a modulation process, which imparts to a sinusoid two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message. For a binary message sequence there are two levels, one of which is typically zero. Thus the modulated waveform consists of bursts of a sinusoid. Figure 2 illustrates a binary ASK signal (lower), together with the binary sequence which initiated it (upper). Neither signal has been bandlimited.

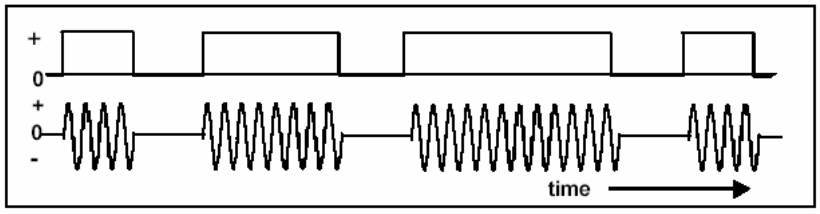

Figure 2: An ASK signal (below) and the message (above)

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There are sharp discontinuities shown at the transition points. These result in the signal having an unnecessarily wide bandwidth. Bandlimiting is generally introduced before transmission, in which case these discontinuities would be 'rounded off'. The bandlimiting may be applied to the digital message, or the modulated signal itself. The data rate is often made a sub-multiple of the carrier frequency. This has been done in the waveform of Figure 2. One of the disadvantages of ASK, compared with FSK and PSK, for example, is that it has not got a constant envelope. This makes its processing more difficult, since linearity becomes an important factor. However, it does make for ease of demodulation with an envelope detector.

BPSK MODULATION

In digital modulation techniques a set of basis functions are chosen for a particular modulation scheme. Generally the basis functions are orthogonal to each other. Basis functions can be derived using 'Gram Schmidt orthogonalization procedure. Once the basis function are chosen, any vector in the signal space can be represented as a linear combination of the basis functions. In Binary Phase Shift Keying (BPSK) only one sinusoid is taken as basis function modulation. Modulation is achieved by varying the phase of the basis function depending on the message bits. The following equation outlines BPSK modulation technique. S0(t)=Acos(ωt)→represents '0'S1(t)=Acos(ωt+π)→represents '1' The constellation diagram of BPSK will show the constellation points lying entirely on the x axis as shown in Figure 3. It has no projection on the y axis. This means that the BPSK modulated signal will have an in-phase component (I) but no quadrature component (Q). This is because it has only one basis function. A BPSK modulator can be implemented by NRZ coding the message bits (1 represented by +ve voltage and 0 represented by -ve voltage) and multiplying the output by a reference oscillator running at carrier frequency ω.

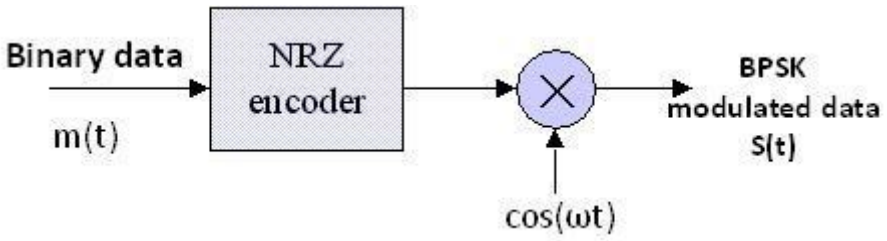

Figure 3: Constellation diagram for modulated BPSK

BPSK DEMODULATOR

For BPSK demodulator, a coherent demodulator is taken as an example. In coherent detection technique the knowledge of the carrier frequency and phase must be known to the receiver. This can be achieved by using a Costas loop or a PLL (phase lock loop) at the receiver. A PLL essentially locks to the incoming carrier frequency and tracks the variations in frequency and phase. For the following simulation, neither a PLL nor a Costas loop is used but instead we simple use the output of the PLL or Costas loop. For demonstration purposes we simply assume that the carrier phase recovery is done and simply use the generated reference frequency at the receiver (cos(ωt)).

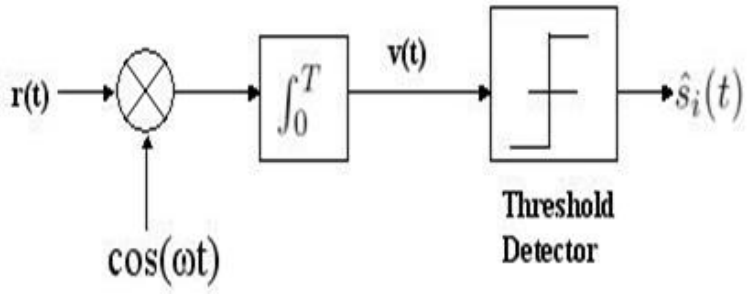

Figure 4: Constellation diagram for Demodulated BPSK

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In the demodulator the received signal is multiplied by a reference frequency generator as shown in Figure 4. The multiplied output is integrated over one bit period using an integrator. A threshold detector makes a decision on each integrated bit based on a threshold. Since an NRZ signaling format is used with equal amplitudes in positive and negative direction, the threshold for this case would be 'o'.

QPSK MODULATION

This modulation scheme is very important for developing concepts of two-dimensional I-Q modulations as well as for its practical relevance. In a sense, QPSK is an expanded version from binary PSK where in a symbol consists of two bits and two orthonormal basis functions are used. A group of two bits is often called a 'dibit'. So, four dibits are possible.

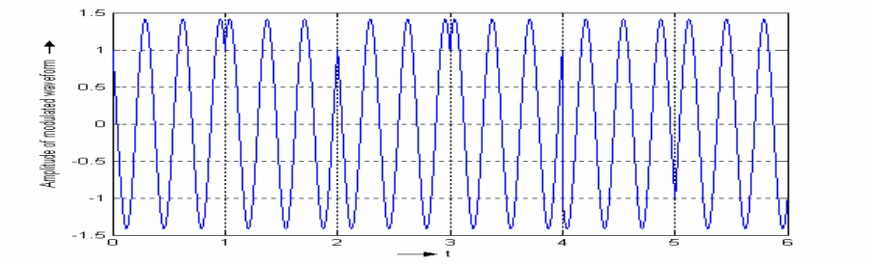

Figure 5: QPSK modulated waveform

Figure 6 shows a schematic diagram of a QPSK modulator. Note that the first block, accepting the binary sequence, does the job of generation of odd and even sequences as well as the job of scaling (representing) each bit appropriately so that its outputs are si1 and si2 . From the observation it is reveal that both the schemes are equivalent while the second scheme allows adjustment of power of the modulated signal by adjusting the carrier amplitudes. Incidentally, both the in-phase carrier and the quadrature phase carriers are obtained from a single continuous-wave oscillator in practice.

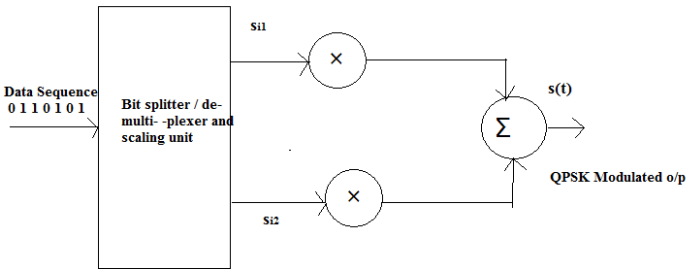

Figure 6: Block schematic diagram of a QPSK modulator

BINARY PHASE SHIFT KEYING (BPSK) AND QUADRATURE PHASE SHIFT KEYING(QPSK)

A very popular digital modulation scheme, binary phase shift keying (BPSK) shifts the carrier sign waves in 180° for each change in binary state as shown in Figure 7.

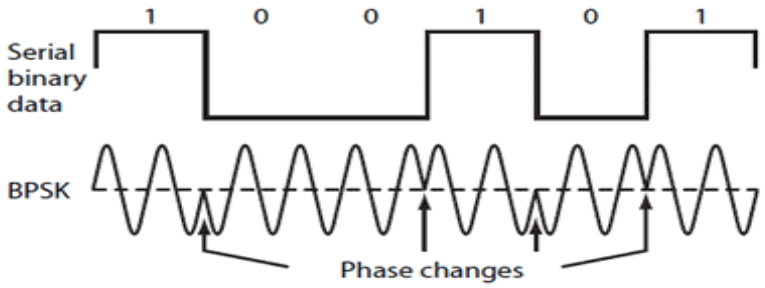

Figure 7: Comparison of BPSK and QPSK

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The simpler version is differential BPSK (or) DPSK where the received bit phase is compared to the phase of the previous bit signal. BPSK is very efficient in that we can transmit at a data rate equal to the band width or 1bit /Hz.In a popular variation of BPSK, quadrature PSK(QPSK) the modulator produce two sine carrier waves 90° apart.The binary data modulates each phase,producing for unique sign signals shifted by 45° from one another. The two phases are added together to shift the final signals.

PROPOSED SIMULATION SOFTWARE TOOLS

The objective of this proposed work is to develop an implementable effective QPSK modulator that uses less power for operation. The design of QPSK modulator has be done using Matlab/Simulink and Xilinx System Generator [9-16]. The modulator algorithm has been implemented on FPGA(Spartan3) using the Verilog Hardware Description Language on Xilinx ISE Design suite 13.2. Then the final designed and simulated results are applied for real time such as Satellite Communication, Video Conferencing etc. This paper presents a method to describe all modulation techniques such as BPSK, ASK, FSK, QPSK, QAM on Field Programmable Gate Array (FPGA) development board which is widely available and inexpensive [17,18]. To develop the system blocks Simulink environment and system generator version 13.1 are used under MATLAB version 7.11 (R2010B).To achieve simulation and synthesis of Spartan 3 FPGA tools from Xilinx ISE 13.1 are used. Very High Speed integrated circuit hardware description language (VHDL) is used for describing the hardware in system understanding language [10].Digital to Analog converter is used to interface both FPGA and CRO which is used to visualize the analog output of the digitally modulated signal**.** The implementation of BPSK modulatorand demodulator couldhave been implemented using Spartan-3 FPGA by using Xilinx ISE 12.1 Project Navigator, Modelsim 6.3, MatlabSimulnk and Xilinx System generator.

RESULTS AND DISCUSSION

Matlab and Simulink algorithm is used to generate code for the designed model. Automatic code is generated due to the library files of matlab and xilink inside the automatic code generation block set. HDL co-simulation is used to combine the hardware and software hence the output of hardware can be obtained with automatic Code generation and not by manual code generation, and also code synthesis, place and route, map, verification of static timing analysis, functional simulation Is also automatically generated. Back annotation is used for the purpose of transferring the verification code to matlab/simulink and then it is connected to the hardware and the output can be generated. The main advantage of this model design is it can be used to implement many hardware like spatron3e, vertex, kintex etc. the schematic diagram for the proposed work as shown in Figure 8.

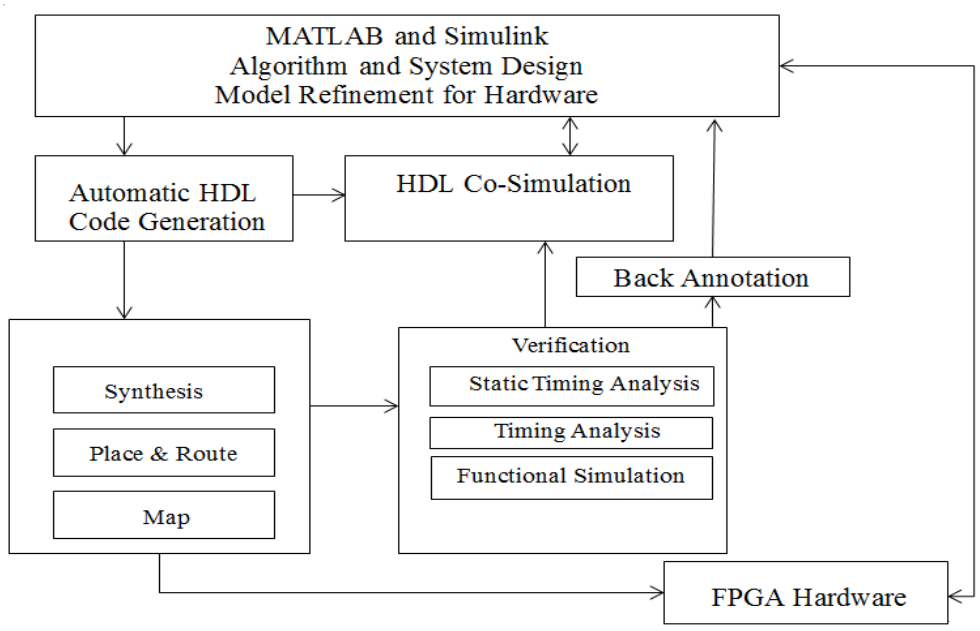

Figure 8: schematic diagram of the proposed work

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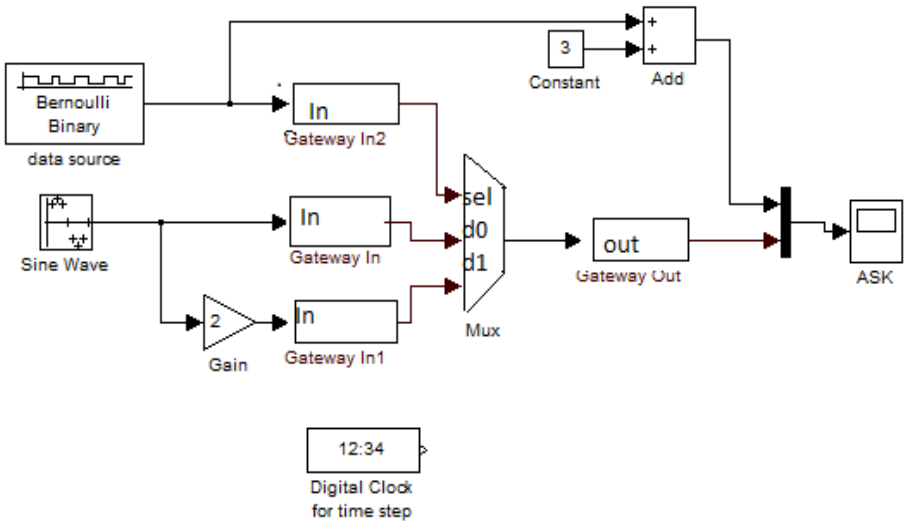

Fiureg 9: Block diagram of ASK modulation

In this block set the Bernoulli binary generator is used as the data source to gateway In2 as shown in Figure 9. In addition to that source sine wave is given to gateway In and gain to gatewayIn1.gateway In convert the simulink data type to system generator data type values. Then the signal is given to multiplexer which combines multiple signal into a single signal and gives the output to gateway out ,which convert system generator data type to simulink data type. Add block is used to add the signal and these two signals combine to generate ASK signal. The code is automatically generated by the use of xilink and matlab as shown in Figure 10.

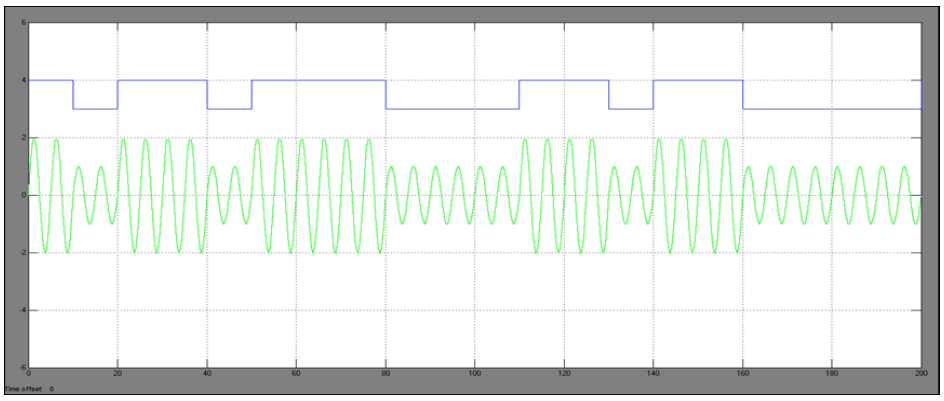

Figure 10: Output waveform of ASK

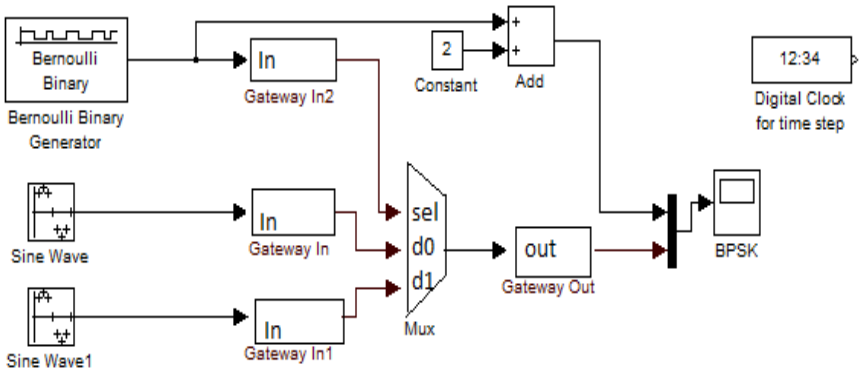

Figure 11: Block diagram of BPSK

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In this block set Bernoulli binary generator and two sine wave signals are given as the input waveform for the gateway In blocks and is given to multiplexer to combine the signal into a single signal and then the output from the gateway out and add block is given to the BPSK block [19-22] in which the signal is generated using simulink / matlab and Xilinx system generator as shown in Figure 11. The corresponding output waveform of BPSK as shown in Figure 12.

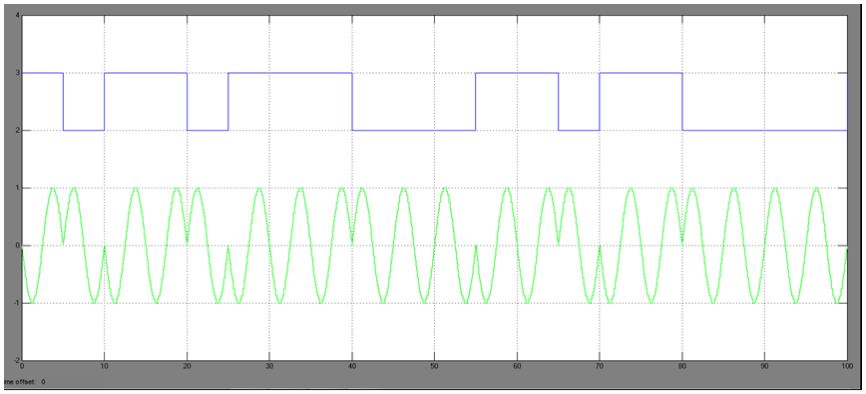

Figure 12: Output waveform of BPSK

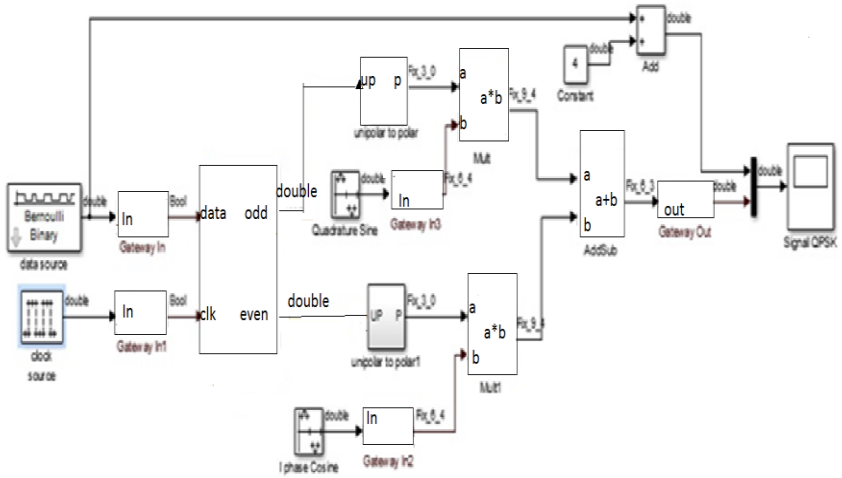

Figure 13: Block diagram of QPSK

- Serial to parallel converter: Series of input of any size and creates a single output of a specified multiple of that size
- Unipolar to Bipolar: The unipolar to bipolar converter block maps the unipolar input signal to bipolar output signal
- Carrier block: Generates the sine and cosine signal
- sum block: It is used to add in phase and quadrature phase signal which results in QPSK modulation signal
- Gateway in: Xilinx gateway in blocks are the inputs into Xilinx portion of your simulation design These blocks convert simulink integer ,double and fixed point data types into the system generator fixed point type.
- Gateway out: Xilinx gateway out blocks are the output from the Xilinx portion This block converts the system generator fixed –point data type into simulink double [23, 24].
- Logical block: It performs bitwise logical operations on 2,3,4 fixed point numbers
- Multiplexer block: It computes the product of the data on its two input ports, producing the result on its output
- Add sub block: The operation can be fixed or changed dynamically under control of the sub mode signal

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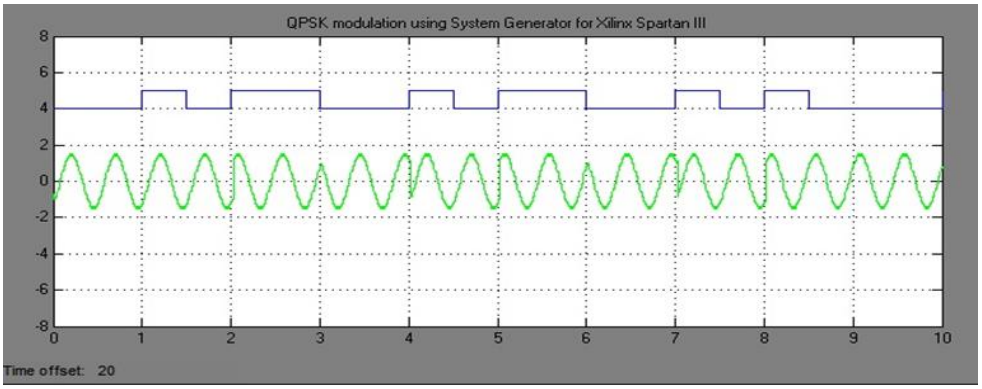

Figure 14: Output waveform of QPSK

Comparison of POWER ANALYSIS OF Existing techniques with proposed Techniques

Table 1 Power analysis of ASK

	Existing method			Proposed method		
On chip	Power(w)	available	utilization	Power(w)	Available	utilization
logic	0.000	66560	0	0.000	7168	0
signals	0.000			0.000		
IOs	0.000	784	2	0.000	141	13
leakage	0.339			0.060		
total	0.339			0.060		

In Existing method the power analysis is done by the lower order modulation technique in which the total power of the system is 0.339 and the proposed method gives the power of 0.060 and hence the power dissipated in proposed method is less than that of the power dissipated in existing method. Table 1 contains power analysis of ASK with existing ones.

Table 2: BPSK Power Analysis

	Existing method			Proposed method		
On chip	Power(w)	available	utilization	Power(w)	Available	utilization
dissipated is 0						
logic	0.000	30720	0	0.000	66560	0
signals	0.000			0.000		
IOs	0.000	448	4	0.000	784	2
DCM's	0.000	8	0			
leakage	0.438			0.339		
total	0.438			0.339		

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Table 2 represents the BPSK powere analysis of proposed method and compared with existing method. In existing BPSK modulation technique the modulation is done by using matlab/simulink and output generated in spatran3e .and the power dissipated is about 0.438 and in proposed method the modulation technique uses the matlab /simulink and xilink system generator software hence due to which the code is automatically generated and the power.339. component utilized by the BPSK device as referred in Table 3.

Table 3: Device utilization of BPSK

	Existing method			Proposed method		
Logic utilization	used	Available	utilization	used	Available	utilization
No . of slice flip flop	97	9312	1%			
No .of 4 I /p LUT's	111	9312	1%	6	30720	1%
No .of occupied slices	94	4656	2%	6	15360	1%
No. Of slices containing only related logic	94	94	100%	6	6	100%
No .of slices containing unrelated logic	0	94	0%	0	6	0%
Total no.of4 i/p flipflop	114	9312	1%	6	30720	1%
No used as logic	111					
No . used as a router	3					
No of bounded IOBS	20	232	8%	19	448	4%
No . Of BUFGMUX's	2	24	8%			
Average fanout of non-clock nets	3.34			1.43		

Table 4: POWER ANALYSIS OF QPSK

	Existing method			Proposed method		
On chip	Power(w)	Available	utilization	Power(w)	Available	utilization
clock	0.004			0.004		
logic	0.001	66560	0	0.001	9312	2
signals	0.001			0.001		
IOs	0.021	784	3	0.025	66	32
leakage	0.340			0.082		
total	0.368			0.113		

In existing QPSK modulation technique the modulation is done by using matlab/simulink and output generated in spatran3e .and the power dissipated is about 0.340 and in proposed method the modulation technique uses the matlab /simulink and xilink system generator software hence due to which the code is automatically generated and the power dissipated is 0.113. The comparison of power analysis of QPSK and device which has utilized the respective components as inferred in Table 4 and 5 respectively.

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Table 5: Device utilization of QPSK

	Existing method			Proposed method		
Logic utilization	used	Available	utilization	used	Available	utilization
No . of slice flip flop	153	7,168	2%	153	3840	3%
No .of 4 I /p LUT's	153	7,168	2%	153	3840	3%
No .of occupied slices	149	3,584	4%	142	1920	7%
No . Of slices containing only related logic	149	149	100%	142	142	100%
No .of slices containing unrelated logic	0	149	0%	0	142	0%
Total no.of4 i/p flipflop	154	7,168	2%	154	3840	4%
No used as logic	69			69		
No . used as a router	1			1		
No of bounded IOBS	22	97	21%	21	173	12%
No . Of BUFGMUX's	1	8	12%	1	8	12%
Average fanout of non-clock nets	1.55			1.55		

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The design summary shows the various synthesizer options that were enabled and some device utilization and timing statistics for the synthesized design.

CONCLUSION

In conclusion the modulation techniques such as ASK, BPSK, QPSK and other higher order modulation can be easily simulated by using matlab/ simulink and xilink system generator. The block set designed in the xilink automatically generate the code from library files and Xilinx. The hardware co-simulation can be achieved through HIL (Hardware-in-loop) and by system generator, which helps to dump the implemented code or generated code into the hardware and to obtain the output. The time saved by working with these types of high level programs is a real advantage. The ASK,BPSK and QPSK System have been designed and implemented successfully in Matlab\Simulink and Xilinx\System Generator and the code generated from system generator has been simulated using ISE 14.3 and FPGA design as well as implemented on many devices like spatran ,vertex, kintex etc. using Verilog Hardware Description Language can be done using this process. The obtained results can be analysed of real time applications such as satellite communication and video conferencing. Of course one of the drawbacks by programming with blocks in general is that the code is not optimized and debugging in a design with a lot of blocks is relatively time consuming and an error is sometimes very hard to find. With normal written code an error can be seen more easily because it is not hidden in a block.

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