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A High Momentum Proficient Adder Designs Using Memristor.

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ABSTRACT

In this paper a new less area, high-speed 1-bit half adder, full adder and ripple carry adder cells are presented. The performance like power time delay and power delay product (PDP) of the proposed Memristor based adder cells has been analyzed in comparison with CMOS based adders. Compare to CMOS based adder design in this proposed Memristor based adders having very less delay in the range of picoseconds. So it will give high speed. In CMOS based design nearly 40 plus transistors has been used to design a adder circuits, but in the case of Memristor based design minimum 10 transistors are used to design a half adder, so area also getting reduced in this proposed Memristor based adder designs. The designs are done in HSPICE environment and delay analysis taken from cosmosscope.

Keywords: Memristance, CMOS, Half Adder, Full Adder, Ripple Carry Adder.

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INTRODUCTION

The Memristor is a new Nano device, a count to the next passive device added, that also includes the resistor, the capacitor and the inductor. Leon O. Chua has found this valuable 4th missed element [1]. A version of the Memristor made-up at Hewlett-Packard Lab in the year of 2008 has a layer of insulating titanium dioxide, TiO2, sandwiched between two platinum (Pt) electrodes. Part of the TiO2 layer is "doped". It has oxygen vacancies that act as positive ions and liberate electrons that can bring an electric current [5]. The overall resistance of the device depends on the position of the boundary between the doped and the undoped regions. This boundary can be move because of a voltage that can apply [2]. Chua theory has nothing to say or other information about the materials and structures of oxygen vacancies. It is formed in terms of the fundamental equations of electric circuits [1,8]. The equations in the four-levels are, voltage, current, charge, and magnetic flux. Each equation establishes a relationship between these two variables. For example, the best-known equation says that Ohm's Law, V = RI. Its excellent resistance into a voltage versus current graph is a straight line slope.

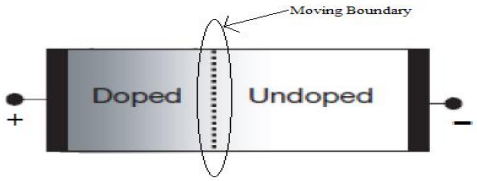

Fig 1: An operation of Memristor with its polarities

At the same format but with different pairs of variables in the equations describing the two basic electrical properties are capacitance and inductance. Two more equations to define the charge and flux based on current and voltage. That makes a total of five equations, which brought together various combinations of four variables voltage, current, charge and flux [2]. Chua observed six possible combinations of four would result in a system that would take a couple of things, so a sixth equation is formulated. Missing Equation charge, magnetic flux is to connect and to describe a new circuit element, that element is called Memristor [3][4].

ADDERS BASED ON CMOS TECHNOLOGY

Since the microelectronics technology available does not advance at the same rate as the Nano technology, digital designers have faced more constraints: high speed, small area, and at the same time, low power dissipation [8][10]. Hence, the research of establishing high recital adder cells is becomes excited. The design of 1 bit full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing to reducing the transistor, reducing the power consumption and increasing the speed.

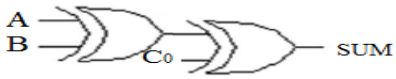

Fig 2a: Logic diagram of half adder

Adder Circuits Using the gates designed using CMOS logic, further extend the circuits towards the basic building block of any computation i.e., adder logic. Adders are used in different configurations to perform addition, subtraction, multiplication or division of bits. In this section reported half adder, full adder and ripple carry adder circuit using CMOS technology. It is shown in the Fig. 2a, 2b, 2c.

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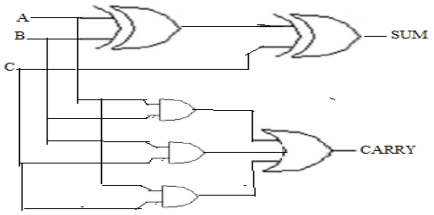

Fig 2b: Logic diagram of full adder

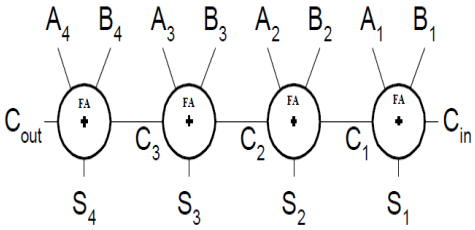

Fig 2c: Logic diagram of ripple carry adder

A Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs [7,9]. Almost every complex computational circuit requires full adder circuitry. The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. Several full adder circuits have been proposed targeting on design accents such as power, delay and area. Among those designs with less transistor count using pass transistor logic have been widely used to reduce power consumption [8,10]. In spite of the circuit simplicity, these designs suffer from severe output signal degradation and cannot sustain low voltage operations [5,9].

MEMRISTOR BASED ADDERS CIRCUITS

The proposed work consists of half adder, full adder and ripple carry adder using Memristor based technology. From the introduction we know all about the Memristor. Compare to Complementary Metal Oxide Semiconductor adder design, the Memristor based adder design is having less area and less delay. Here the number of transistor used for design the adder is less when compare to other. For replacing the Memristor in the place transistor we are getting better results. The design of half adder, full adder, ripple carry adder and its operation is given below. The basic inverter and nor gate designs are shown in Fig.3 and Fig.4.

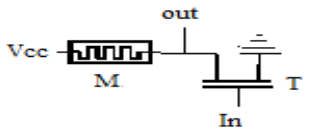

Fig 4: Basic inverter using Memristor

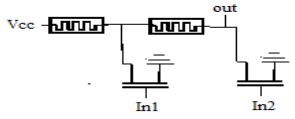

Fig 5: NOR gate using Memristor

HALF ADDER

In this proposed design Memristor based half adder has been designed. It consists of ten Memristors and ten MOSFETs. M indicate the Memristor and T indicates the MOSFET.

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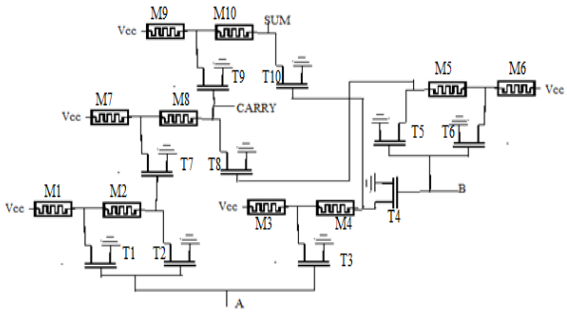

Fig 6: Proposed half adder design using Memristor

Here M1, M3, M6, M7, M9 are connected in to Vcc. First input of the half adder is given to the MOSFETs T1, T2, T3(interconnected), second input of the half adder is given to the MOSFETs T5, T6, T7(interconnected), sum output of half adder is taken from Memristor M10 and the carry out is taken from in between MOSFET T9 and Memristor M8. Depends up on the input signal the operation of half adder is working. Outputs are verified by the use of truth table of half adder.

FULL ADDER

In this proposed Full adder design consists of 24 Memristors, 24 MOSFETs. In Memristor there is no voltage drop for a particular frequency. After some frequency some voltage drop may occur, so cannot able to connect more number of Memristor in series manner. The below Figure 7 is the proposed design of full adder using Memristor. Usually in cmos technology based adder circuits consist of more number of transistors so because of long wiring process parasitic effect is occurring so power and delay is getting increased. To avoid this problem moving for Memristor based adder design. The sum output is basically obtained by a cascaded XNOR of the three inputs in accordance with above mentioned equation of full adder. The carry output is obtained in accordance with above mentioned equation. The final sum of the products is obtained using a wired XNOR logic. Figure 7, shows the full adder circuit design using Memristor based technology.

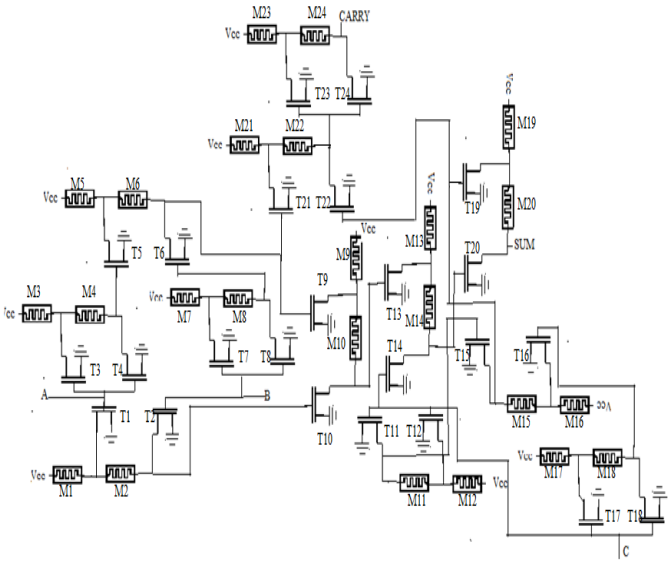

Fig 7: A Proposed full adder design using Memristor

Figure 7 tells about the Memristor based full adder design and its operation. The results are verified by the use of truth table which is given above in adder's explanation.

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RIPPLE CARRY ADDER

In this proposed RCA design consists of four Memristor based full adder. Simply say that four full adders are connected in cascaded manner. It is a n bit adder. Each sum value is depends on the previous carry value. The critical path of the design is goes from Cin to Cout. Ripple Carry Adder is one of the fast adders. In this Memristor based RCA design we will get less area and less delay so can prefer Memristor based digital circuits for designing a digital circuits. And also reduce the power delay product. Area is reducing means automatically speed will also get increase. This proposed RCA design is cascading of four Memristor based full adders. And each carry of the one full adder is propagating in to the next full adder and the sum outputs are taken from each full adder stages.

RESULTS AND DISCUSSION

In this paper Memristor based half adder, full adder and ripple carry adder has been designed. The half adder, full adder and ripple carry adder are designed and simulated in HSPICE environment. The results are compared with conventional CMOS design. The area and delay are getting reduced because of Memristor effect. The output wave forms of basic inverter using Memristor, nor gate design using Memristor, half adder, full adder and ripple carry adder design using Memristor are given in the below figures. From the figure we will get the proper response of the proposed design.

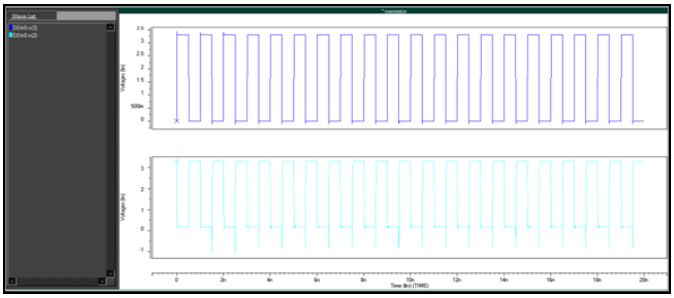

Fig 8: Output wave form of basic inverter using Memristor

Fig. 8 describes the transient analysis of inverter. In this analysis v(3) represent the input signal and v(2) represent the output signal

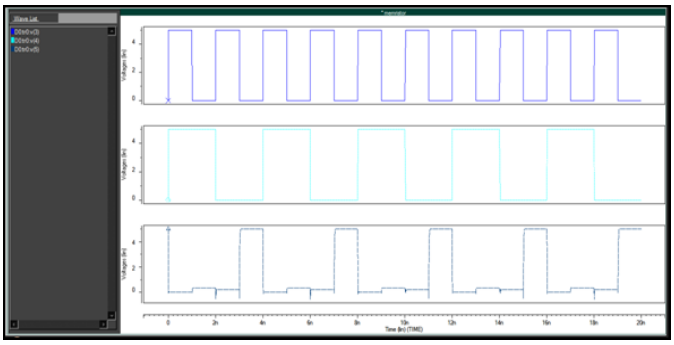

Fig 9: Output wave form of NOR gate using Memristor

Fig. 9 describes the transient analysis of NOR gate. In this analysis v(3), v(4) represents the input signals and v(5) represents the output signal.

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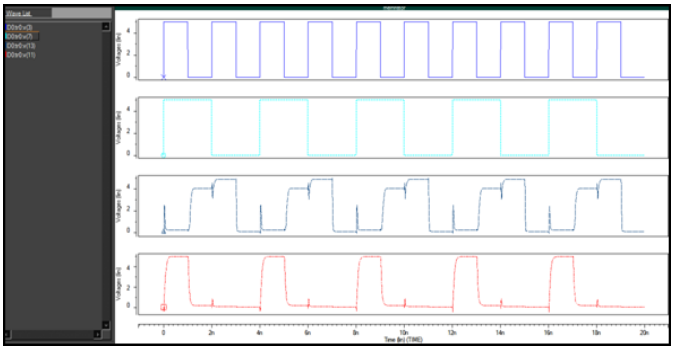

Fig 10: Output wave form of half adder using Memristor

Fig 10 describes the transient analysis of half adder. In this analysis v(3), v(7) represents the input signals and v(13), v(11) represents the output signals.

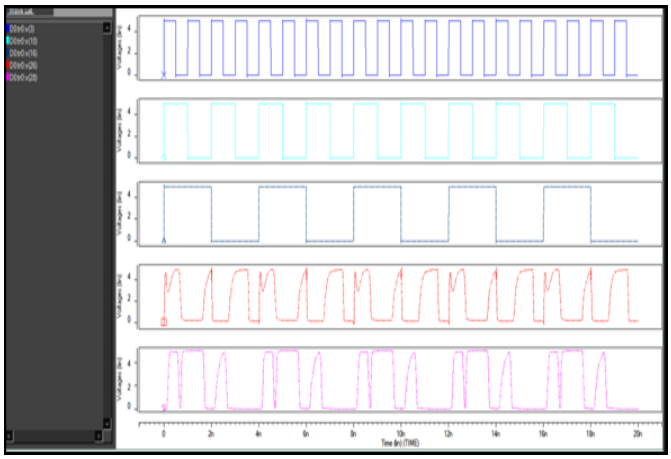

Fig 11: Output wave form of full adder using Memristor

Fig 11 describes the transient analysis of full adder. In this analysis v(3), v(10), v(16) represents the input signals and v(26), v(28) represents the output signals.

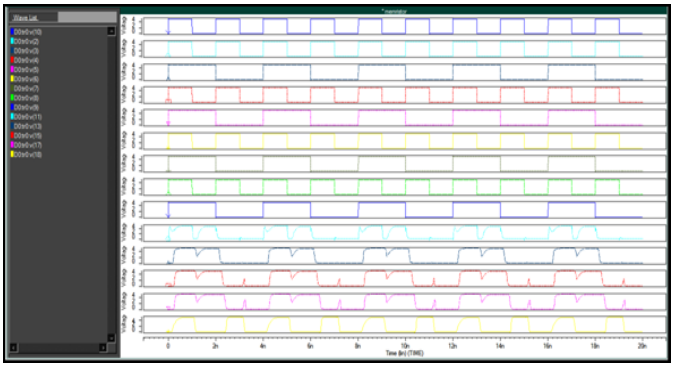

Fig 12: Output wave form of RCA using Memristor

Fig. 12 describes the transient analysis of RCA. In this analysis v(10), v(2), v(3), v(4), v(5), v(6), v(7), v(8), v(9) represents the input signals and v(11), v(13), v(15), v(17), v(18) represents the output signals Figure 11 shows the simulated waveforms of full adder using Memristor model, where first two wave forms are inputs and next wave form is sum output and the last wave is the carry output. By the use of truth table we can analysis the performance of the proposed Memristor based Full adder design. For example for (1 1) combination we are getting zero as sum value and one is the carry output. The output wave form of Ripple

Carry Adder is shown in the fig. 12. The waveforms are taken from HSPICE (Avanwaves A-2008.03) tool and the power consumption values are noted and given in to the comparison table.

The Table-1 describes the performance analysis of COMS and Memristor technology based design of multiplexers.

TABLE I: COMPARISON TABLE FOR BOTH CMOS AND MEMRISTOR TECHNOLOGY

Designs	CMOS Technology		Memristor Technology	
	Total No. of Transistors	Delay (s)	Total No. of Transistors	Delay
Half Adder	20	1.088 n	10	20.89 p
Full Adder	48	105.16 p	24	21.692 p
RCA	192	1.259 n	96	269.7 p

CONCLUSIONS

In this paper, half adder, full adder and ripple carry adder has been implemented, simulated and analysed using Memristor model. Here observed that compared to conventional CMOS based design, hybrid Memristor based design have less power consumption and speed is also high. So Memristor based basic adder and fast adder designs can prefer for any digital design which is having adder as a component. So it will reduce the area and increase the speed for higher level of digital designs. Future scope by the use of this model we can implement Adder based digital designs.

REFERENCES

[1] L. O. Chua and S. M. Kang, “Memristive Devices and Systems,”Proceedings of the IEEE, Vol. 64, No. 2, pp. 209- 223, February 1976.S.

[2] P. Vontobel, W. Robinett, J. Straznicky, P. J. Kuekes, and R. S. Williams, “Writing to and Reading from a Nano-Scale Crossbar Memory Based on Memristors,” Nanotechnology, Vol. 20, No. 42, pp. 1-21, October 2009.

[3] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The Impact of Gate-Induced Drain Leakage Current on MOSFET Scaling," Proceedings of the IEEE International Electron Devices Meeting, pp. 718-721, December 1987.

[4] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Procedure," Proceedings of the IEEE International Conference on Computer Design, pp. 142-147, October 2011.

[5] Shahar Kvatinsky, Nimrod Wald, Eby G. Friedman,” MRL– Memristor Ratioed Logic,” "Heterogeneous Computing, the Inevitable Solution: Power Management, Scheduling and ISA," Grant no. 864-737-13.2010.

[6] Joy Chowdhury, 2j. K. Das, 3n. K. Rout,” Implementation Of 24t Memristor Based Adder Architecture With Improved Performance,” Proceedings of 23rd IRF International Conference, Pune, India, ISBN: 978-93-82702-84-9, 29th March 2015

[7] Vingtao jiang, abdulkarim al-sheraidah,yuke wang, edwin sha, and jin-gyun chung, “a novel multiplexer-based lowpower full adder”, ieee transactions on. circuits and systems—ii: express briefs, vol. 51, no. 7, july 2004.

[8] Ravi.T “Design and performance analysis of ultra low power RISC processor using hybrid drowsy logic in CMOS technologies” International Journal of Applied Engineering Research (IJAER) Volume 10, Number 2 (2015) pp. 4287-4296

[9] S.Ranjith, T.Ravi, P.Umarani, R.Arunya ”Design of CNTFET based sequential circuits using fault tolerant reversible logic” International Journal of Applied Engineering Research Volume 9, Number 24 (2014) pp. 25789-25804

[10] M.Micheal Priyanka, T.Ravi, ”Survey on Role of Memristor in Electronics Devices”, International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), 978-1-4673-9825-1/15/$31.00 ©2015 IEEE , pp. 738-744, 2015.

[11] Mariano Aguirre-Hernandez and Monico Linares-Aranda," CMOS full adders for energy efficient arithmetic application", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 4, April 2011
[12] Kyung Hyun Choi and Muhammad Naeem Awais," Cost-effective Printed Memristor Fabrication and Analysis,"978-1-61284-857- 0/11/$26.00 ©2011 IEEE
[13] Vahid Foroutan and Keivan Navi," Low Power dynamic CMOS full adder cell", Vahid Foroutan et al, / (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 6 (3) , 2015, 3198-3201.
[14] "High performance multipliers," IEEE Journal of Solid- State Circuits, Vol. 31, No. 10, pp. 1535-1546.
[15] Ms.G.L.Madhumati, Dr.M.Madhavilatha, and Mr. K. Ramakoteswara Rao, "Power and Delay Analysis of a 2-to-1 Multiplexer Implemented in Multiple Logic Styles for Multiplexer-Based Decoder in Flash ADC", International Journal of Recent Trends in Engineering, Vol. 1, No. 4, May 2009.