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Performance Analysis of an Efficient D Flip-Flop Based Linear Feedback Shift Register Using CMOS Technology

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ABSTRACT

In this paper, average power, delay, power delay product and leakage feedback technique is applied for linear feedback shift registers. The design of low-power digital system is crucial using low power flip-flops. As Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are minimized to ranges which are in nanometer and Complementary MOS (CMOS) circuit's total Power consumption is given a new definition. In today's world leakage power tends to play a major role in total power consumption due to the integration of millions of components and shrinking process technology. In this paper, the linear feedback shift registers are designed and their performances are analyzed.

Keywords: Flip-flops, Single event upset, LFSR, CMOS technology.

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INTRODUCTION

A flip-flop has two stable states and it is used for storing state information. In sequential logic,it acts a basic storage element. A DFF is called as a Delay or Data flip flop which has one data input D and a clock. The output takes the state of D input at the moment of positive edge at the clock pin or negative edge if the clock input is active low and delays it by one clock cycle. LFSR is a shift register whose input bit is a linear function of its previous state and it is driven by an exclusive OR gate. The initial value of LFSR is called the seed where the stream of values produced by the register is completely determined by its current or previous state since the operation of the register is deterministic. It is used to generate pseudo random numbers. Shift register is a cascade of flip-flop where these flip-flops shares the same clock. These cascade of flip-flops are connected in a chain where the output of one flip-flop becomes the input of the next flip-flop [5]. Shift register is a type of sequential logic circuit mainly used for the storage or transfer of data in the form of binary numbers. Shift registers can have both parallel and serial inputs and outputs and these can be classified into

- Serial-in serial-out
- Parallel-in serial-out
- Serial-in parallel-out
- Parallel-in parallel-out.

In serial-in serial-out, the data's are serially fed into the shift registers as inputs. The flip-flops shifts the data one bit at a time and produces the stored information as the output in serial form. In serial-in parallel-out, the serial in parallel out is similar to that of serial in serial out. The data's are serially fed into the shift registers as inputs where the outputs are produced at the respective flip-flops parallel. In parallel-in serial-out, the data inputs are fed into the shift registers through the data lines parallel. But the stored information's are produced serially at the output. In parallel-in parallel-out, the shift registers accepts the data as the input in parallel form. The flip-flops immediately produce the data at the output line simultaneously in parallel form.

EXISTING SYSTEM

A conventional master-slave flip-flop is a very sensitive flip-flop when a particle strikes; it causes a Single Event Upset (SEU). When a clock is either high or low, SEU may upset the logic state of the master and slave latch resulting in a faulty output where erroneous value will be locked in the slave latch when the clock is low[7].Using dynamic logic, SEU in the master or slave latch of a flip-flop can be detected by an error detection circuit. According to the error detection signal the multiplexer selects the correct output. A SEU hardened flip-flop includes a data input D and two complementary clock signals clk and clk-bar. When clock is low and clock bar is high, the transmission gate T0 is enabled and T1 is disabled where the logic state on the data input D is written into the master latch. When the clock signal changes from low to high, it allows the master slave to store the data input value. The data input value is locked in the master latch when the clock signal goes high (clock bar low) where the transmission gate T0 is disabled and T1 is enabled. Simultaneously when the clock changes from low to high, the transmission gate T2 is enabled and T3 is disabled which allows the signal captured at the rising edge of the clock to pass through the slave latch. The output Q of the slave latch is locked when there is a transition from high to low in the clock signal, the transmission gate T2 is disabled and T3 is enabled. The value obtained at the last rising edge of the clock is held while the master latch begins to accept the new values in preparation for the next rising clock edge.

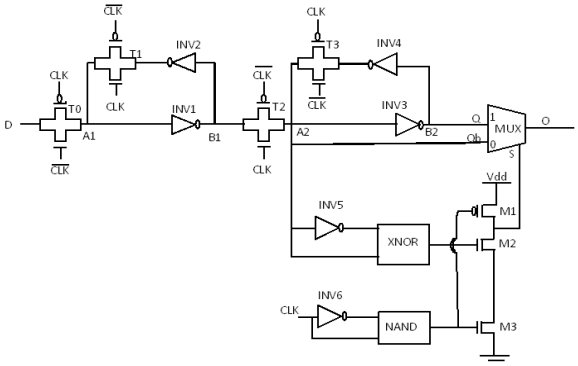

Figure 1: SEU Hardened FlipFlop

During the hold phase of the master latch, SEU on node A1 or B1 may upset the logic state of this master latch resulting in a faulty output Q. The erroneous value will also be locked in the slave latch when clock is low. During the hold phase of the slave latch, SEU on node A2 or B2 may upset the logic state of the slave latch also results in a faulty output Q. The SEU hardened flip-flop can mitigate SEU during the whole clock period. An error detection circuits is used to detect SEU in the master latch and the slave latch[7]. The resultant fault indication signal S selects the correct value on node Q or Qb as the final output. The hardened flip-flop has one error detection circuit and one multiplexer which introduces small area and performance overheads.

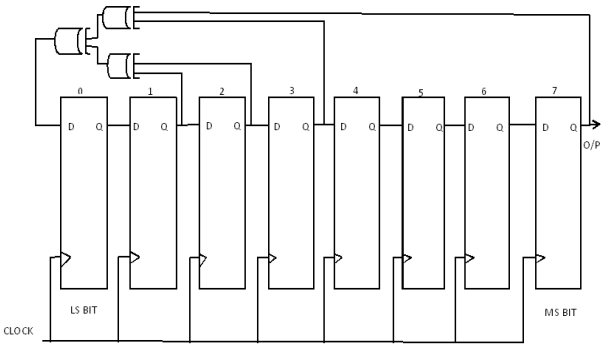

Figure 2: Linear Feedback Shift Register

PROPOSED SYSTEM

The Low Power D- flip-flop is basically a Master Slave flip-flop structure. Figure.3 shows the low power d flip-flop and this flip-flop consists of two data paths. The n-type pass transistors basically gives weak high but in figure 3, the n-type pass transistors are followed y an inverter, which results in strong high from figure3, the low power d flip-flop is free from threshold voltage loss problem of transistors. Therefore low power D flip-flop has become more efficient in terms of area, power and speed which claim better performance than conventional designs. The conventional D flip- flop in the linear feedback shift register is replaced with modified D flip-flop.

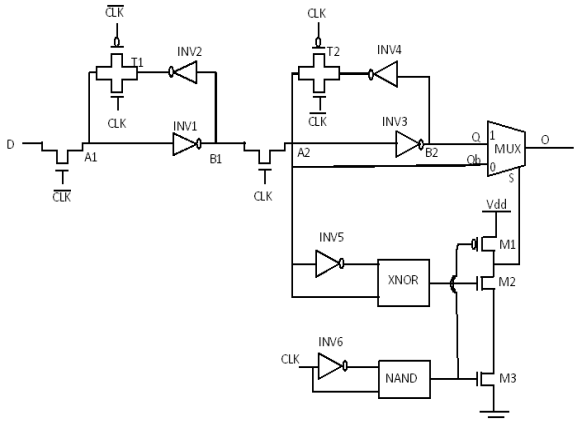

Figure 3: Modified FlipFlop

LFSR is a linear feedback shift register which has a conventional D flip-flop. In this paper, we have proposed a modified SEU hardened flip-flop. This SEU hardened flip-flop is replaced in place of the conventional D flip-flop. The power, delay, power delay product are compared with the existing system.

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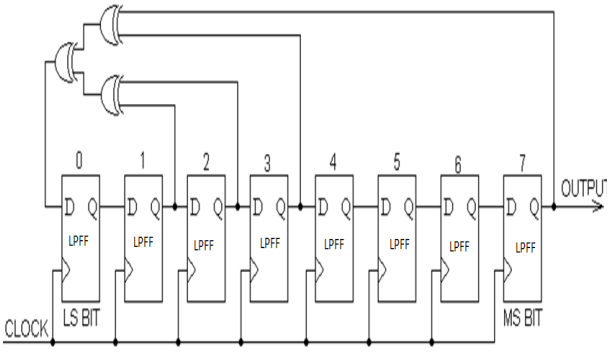

Figure 4: Modified LFSR

SIMULATION RESULTS

To evaluate the performance, shift registers discussed in this paper are designed using 130-nm CMOS technology. The simulations are carried out using HSPICE simulation tool.The simulated waveform of linear feedback shift register is shown in Figure.5 and Figure.6.

Figure5. Represents the modified D flip-flop waveform where v(25) is the input clock pulse and v(2) is the input pulse. The v(100) is the delayed output.

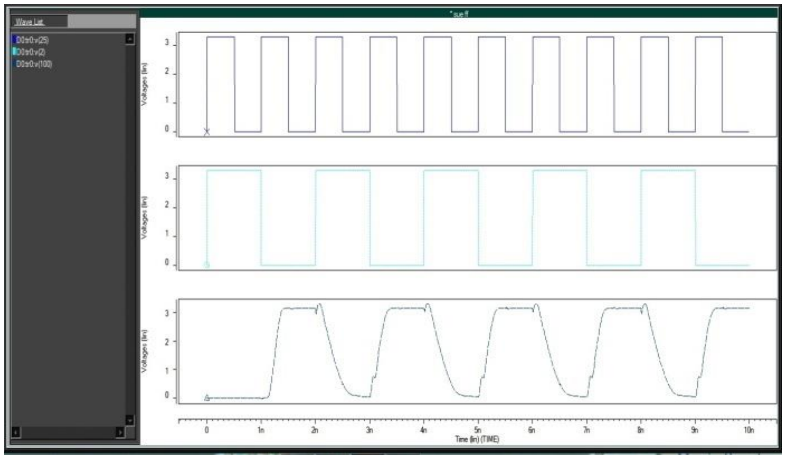

Figure 5: Modified DFF

Figure 6. Represents the modified LFSR where v(2) is the clock pulse and v(3) is the input signal. The input waveform is delayed for every clock signal and the outputs are obtained for each flip-flop.

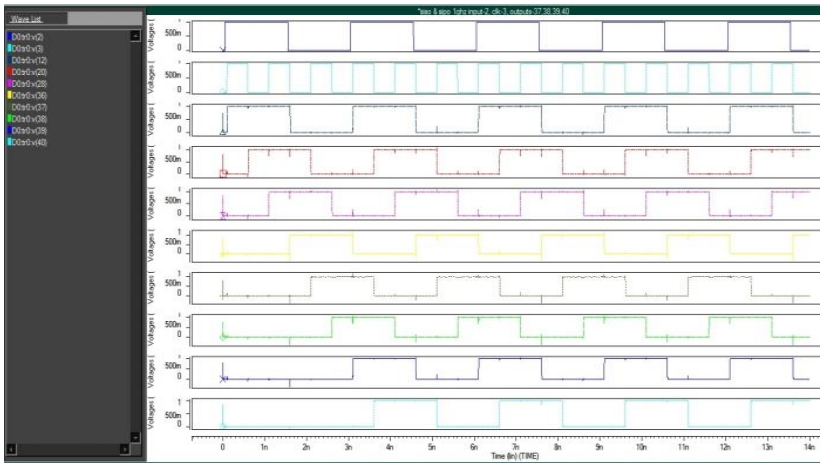

Figure 6: Modified LFSR

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PERFORMANCE ANALYSIS

TABLE 1: COMPARISON TABLE FOR DFF AND MDFF

DEVICE	POWER	DELAY	POWER DELAY PRODUCT
DFF	23.78µW	10.374ps	0.246fJ
MDFF	17.06µW	7.1528ps	0.122fJ

From the comparison shown in the Table.1, Modified DFF has minimum Delay, Power and power delay product.

TABLE 2: COMPARISON BETWEEN LFSR AND MLFSR

DEVICE	POWER	DELAY	POWER DELAY PRODUCT
LFSR	0.787mW	9.21ps	7.247fJ
MLFSR	0.641mW	8.45ps	5.418fJ

Table 2 shows the comparison between linear feedback Shift Register and modified FFSR. From the Result we can conclude that MLFSR has less power when compare to LFSR.

TABLE 3: COMPARISON OF LEAKAGE FEEDBACK TECHNIQUE BETWEEN LFSR AND MLFSR

DEVICE	POWER	DELAY	POWER DELAY PRODUCT
LFSR	1.972mW	10.558ps	20.82fJ
MLFSR	1.390mW	9.10ps	12.649fJ

Table 3, shows the comparison of Leakage feedback technique between linear feedback shift Register and Modified Linear Feedback Shift Register. When comparing to the Linear Feedback Shift Register MLFSR shows great improvement in Delay and also in PDP.

PERFORMANCE CHART

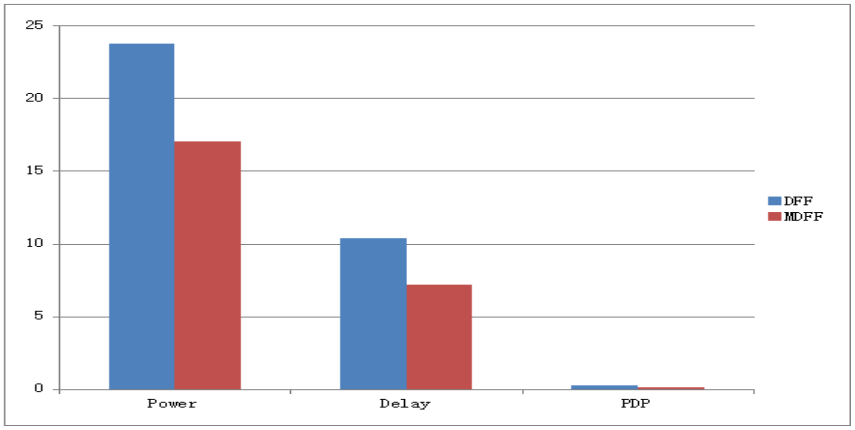

Figure 7: DFF vs. MDFF

Figure 7 shows the Power, Delay and PDP comparison between D Flip Flop and Modified D Flip Flop.

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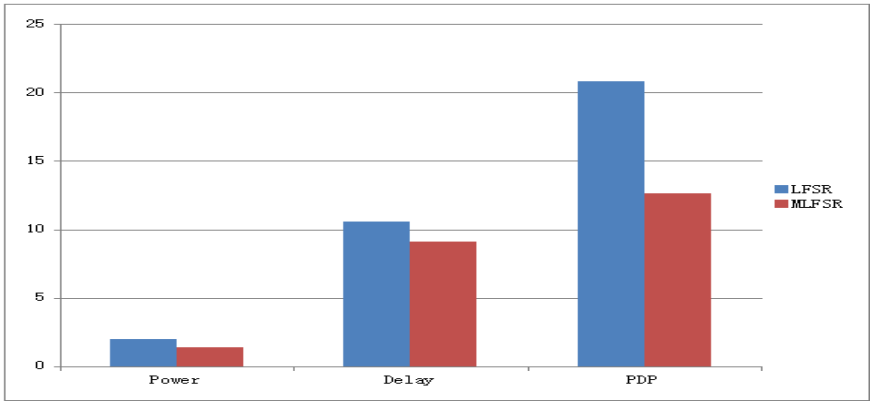

Figure 8: LFSR vs. MLFSR

Figure 8 shows that the proposed LFSR has lowest PDP. It gives 50% reduction in power dissipation when compare to the existing LFSR.

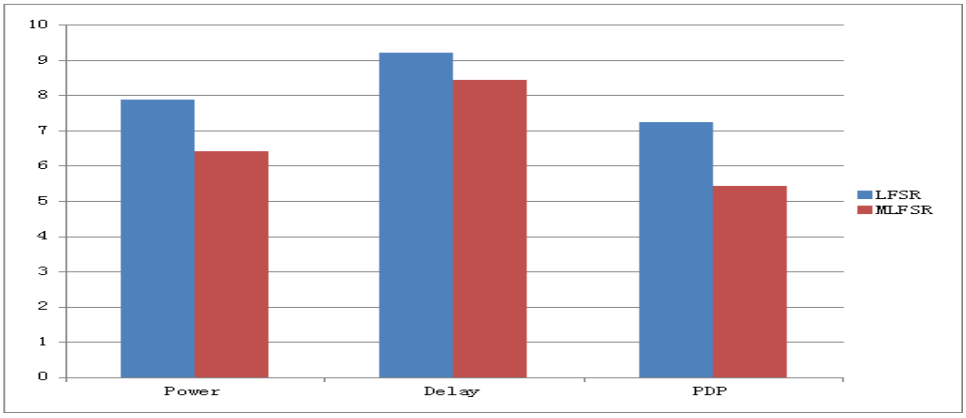

Figure 9: Comparison of Leakage Power Technique between LFSR and MLFSR

Figure 9 illustrate the comparison of leakage power technique between LFSR and MLFSR. We observe that LFSR is the worst, whereas MLFSR achieve higher performance.

CONCLUSION

In this paper, it has been designed D-FF based linear feedback shift registers design in 130nm CMOS technology. The linear feedback shift registers are simulated with different operating frequencies ranging from 100MHz to 1GHz.The linear feedback shift registers design is efficient by comparing average power, delay and power delay product. Hence by performance analysis the D-FF based linear feedback shift registers design is efficient for low power applications.

REFERENCES

[1] DejanMarkovic, BoribojeNikolic and Robert.W.Brodersen, " Analysis and design of Low energy flip-flops", Berkeley Wireless Research center, University of California, Berkeley, 2000

[2] K. Namba, T. Ikeda, and H. Ito, "Construction of SEU tolerant flipflops allowing enhanced scan delay fault testing," IEEE Trans. Very LargeScaleIntegr.(VLSI)Syst.,vol.18,no.9,pp.126 5 1276,2010.

[3] Markovic.D, B.Nikolic, B.G.Oklobdz(2000), " A general method in synthesis of pass transistor circuit," Microelectronics Journal 31, pp-1991-1998.

[4] N.Mathan, T.Ravi and E.Logashanmugam, "Design and analysis of low power single edge triggered D flip-flop based shift registers,"IJETAE, vol.3, issue 2,Feb.2013.

[5] N.Mathan, "CNTFET Based highly durable radix-4 multiplier using an efficient hybrid adder", Bio Sciences Biotechnology Research Asia, Dec.2014, vol.11(3),pp 1855-1860.

[6] SheXianoXuan,N.Li and J. Tong, “SEU hardened flip-flop based on dynamic logic,” IEEE trans.on nuclear science.Rel.,vol.60,no.5 oct. 2013.
[7] Vladimir Stojanovic and Vojin G. Oklobdzija," Comparative Analysis of Master–Slave Latches and Flip-Flops for High-Performance and Low-Power Systems.
[8] X. She, N. Li, and J. Tong, “SEU tolerant latch based on error detection,” IEEE Trans. Nucl.Sci, vol.59,no.1,pp.211-214, Feb.2012
[9] Yeo.K and Roy.K“Low voltage , low power VLSI subsystem” McGraw-Hill publication 1998.
[10] N.Mathan, “CNTFET Based highly durable radix-4 multiplier using an efficient hybrid adder”, Bio Sciences Biotechnology Research Asia, Dec.2014, vol.11(3),pp 1855-1860.
[11] V.Santhiya and N.Mathan, “Performance Analysis Of An Energy Efficient FFT Processor Using 32nm CMOS Technology”, ARPN Journal of Engineering and Applied Sciences, June.2015, vol.10(10),pp 4456-4461.
[12] J.Elakkiya and N.Mathan, “Highly Reliable Low Power Mac Unit Using Vedic Multiplier”, ARPN Journal of Engineering and Applied Sciences, June.2015, vol.10(10),pp 4557-4562.